Technical Product Description
SMA131

Triaxial Accelerometer for Non-Safety Automotive Applications

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Table of Contents

1 Product Identification

- Product Designation: SMA131
- Type Designation: Accelerometer
- Product Part Number: 0273 141 290
- This Product is intended for use in: Non-Safety Automotive Applications

1.1 Main Functions and Properties

The SMA131 is a triaxial, low-g accelerometer for non-safety related wake-up functionality applications. Within one package, the SMA131 offers the detection of acceleration in three perpendicular axes. The digital standard serial peripheral interface (SPI) of the SMA131 allows for bi-directional data transmission.

1.2 Key Features

Key Features	Description
Triaxial accelerometer	Versatile, leading edge triaxial 14 bit accelerometer for reduced PCB space and simplified signal routing
Small package	LGA, 12 pins, footprint 2.0 x 2.0 mm², height 0.95 mm
Common voltage supplies	VDD voltage range: 1.62 ... 3.6 V
Digital interface	SPI, TWI (compatible with I^2C), 2 interrupt pins
Consumer electronics suite	MSL1, RoHS compliant, halogen-free
Operating temperature	-40 ... +85 °C
Extended operating temperature	-40 ... +105 °C (details see chapter 5.2)
Programmable functionality	Acceleration range selectable Low-pass filter bandwidths selectable
Ultra-low power	Low current consumption, several power saving modes
On-chip interrupt controller	Motion-triggered interrupt signal generation for high-g detection no-motion / slow-motion detection slope / any-motion detection new data detection

2 General Product Description

2.1 Mechanical Design

The accelerometer SMA131 consists of an evaluation circuitry (ASIC) and a micro-mechanical sensing element (MEMS) within a standard LGA package. The read out ASIC is stacked on top of the respective sensing element.

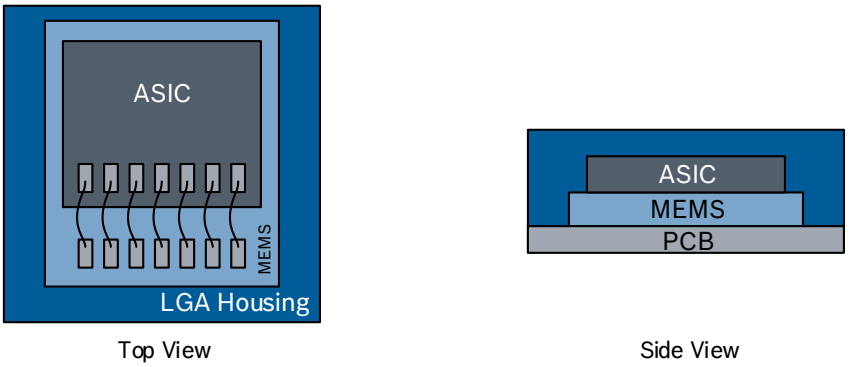


Figure 1 Schematics of the SMA131 mechanical design (left: top view; right: side view)

2.2 Sensor Data

The settings for the accelerometer has to be set during startup. The detailed description can be found in section 7.1. How to read and evaluate the sensor data is described in section 7.6.

For the sensing element it is recommended to actively set an appropriate, application specific bandwidth between 7.81 Hz and 1000 Hz. Similar to the bandwidth, the measurement range can be selected by a specific register setting. The measurement range for the accelerometer is from ±2 g to ±8 g.

The data representation follows two´s complement representation. For each axis, the acceleration data is split into a MSB upper part and a LSB lower part. It is recommended to always start with reading the LSB register.

In order to ensure data integrity, a **shadowing procedure** can be enabled. When this is enabled, the content of the MSB register is locked when reading the corresponding LSB register, until the MSB register is read. This means that the MSB register always has to be read in order to remove the data lock. Shadowing can be disabled or enabled for each sensing part separately. For disabled shadowing, the content of both MSB and LSB registers is updated immediately.

Two different streams of acceleration data are available, **unfiltered** and **filtered** data. The unfiltered data is sampled with 2 kHz. The sampling rate (output data rate ODR) of the filtered data depends on the selected filter bandwidth (BW). Based on the specific register settings, either the filtered or unfiltered data is stored in the registers.

2.3 Block Diagram

Figure 2 shows the basic building blocks of the SMA131. An acceleration signal along the sensitive axis of the MEMS element causes a change of the capacitances of the MEMS element. This change is converted into a digital serial bit stream which is further processed and which can be accessed via SPI or TWI.

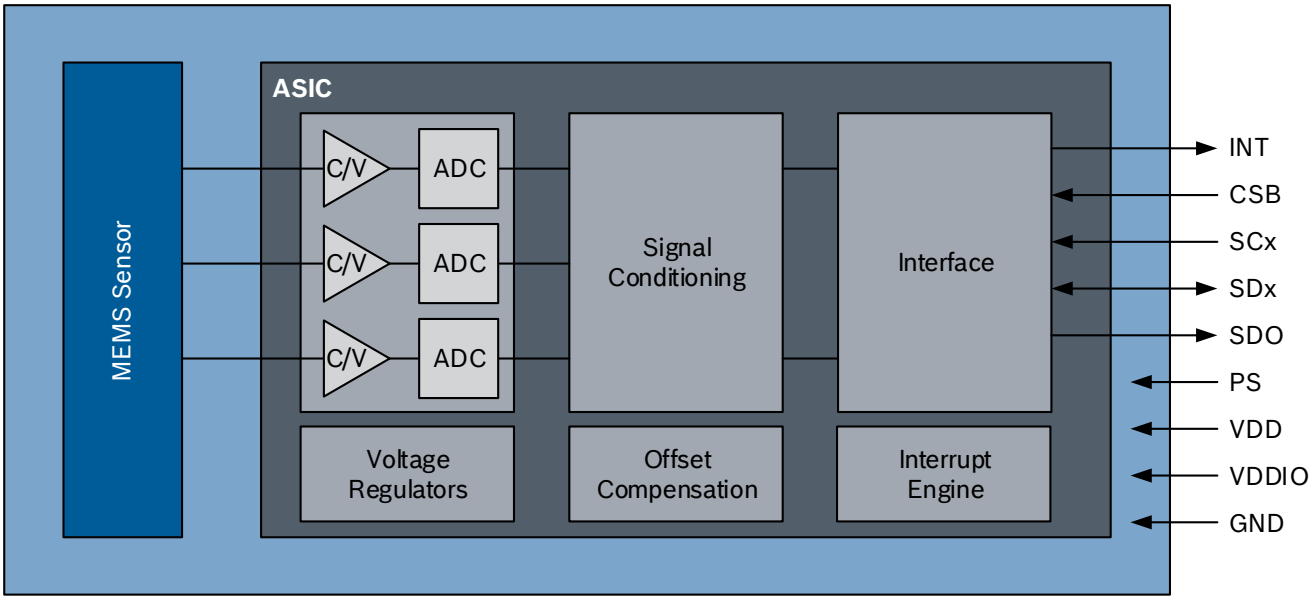


Figure 2 Simplified block diagram of the SMA131

2.4 Signal Path

The SMA131 offers acceleration data for all three spatial dimensions. For the latter, the differential capacitance change (C) of the corresponding sensing element is detected. This signal corresponds to the voltage (V) entering the hybrid algorithmic analog-digital-converter (ADC), translating the formerly analog signal into a digital serial bit stream at a rate of 400 kHz. Then, the detected signal is translated into a data word of 14 bit and enters the digital signal processor (DSP).

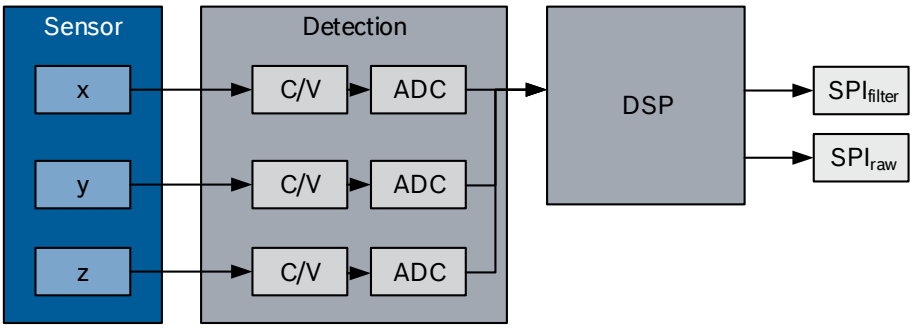


Figure 3 Simplified signal path of the SMA131

Within the DSP (see Figure 4), the data is corrected for the analog-digital conversion, gained and offset corrected. A low-pass filter engine provides an adjustable data bandwidth. Here, the sampling rate is directly connected with the selected bandwidth.

The low-pass engine can be bypassed so that unfiltered data is accessible.

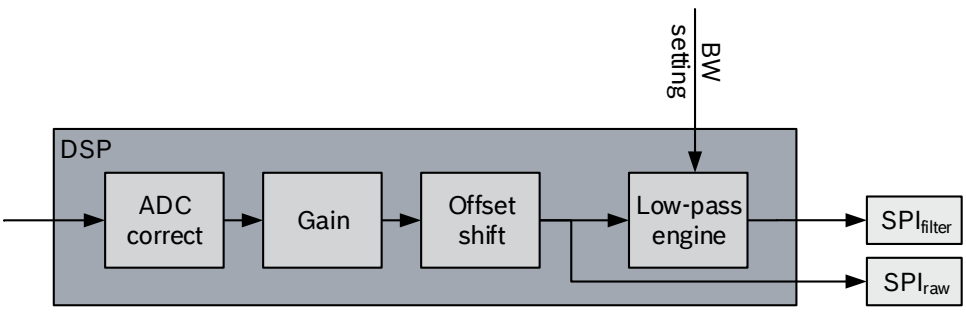


Figure 4 Simplified DSP element

2.5 Orientation of the Sensing Axes

If the sensor is accelerated in the sensing directions indicated in Figure 5, the corresponding channels of the device will deliver a positive acceleration signal (dynamic acceleration). If the sensor is at rest and the force of gravity is acting along the indicated sensing directions, the output of the corresponding acceleration channels will be negative (static acceleration).

Example:

If the sensor is at rest or at uniform motion in a gravity field according to Figure 5, the output signals are

- ±0 g for the x-channel,
- ±0 g for the y-channel and
- +1 g for the z-channel.

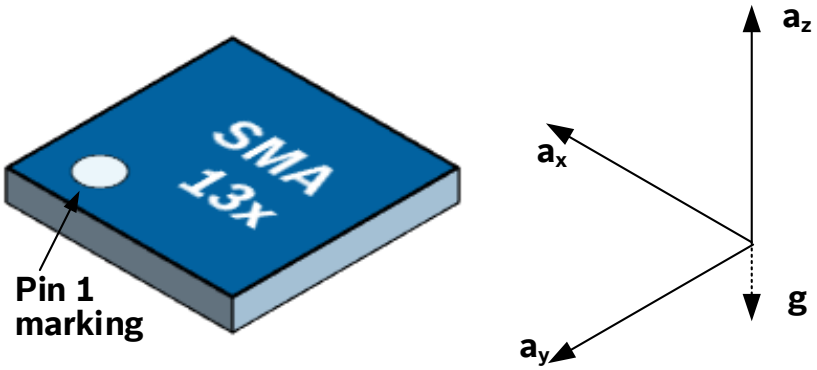


Figure 5 Orientation of the sensing axes

The table below lists all corresponding output signals on x, y and z while the sensor is at rest or at uniform motion in a gravity field under assumption of a ±2 g range setting and a top down gravity vector as shown above.

Sensor orientation (gravity vector ↓)	SMA 13x Earth	SMA 13x Earth	SMA 13x Earth	SMA 13x Earth	Earth	Earth
Output signal x	0 g 0 LSB	1 g 4096 LSB	0 g 0 LSB	-1 g -4096 LSB	0 g 0 LSB	0 g 0 LSB
Output signal y	-1 g -4096 LSB	0 g 0 LSB	1 g 4096 LSB	0 g 0 LSB	0 g 0 LSB	0 g 0 LSB
Output signal z	0 g 0 LSB	0 g 0 LSB	0 g 0 LSB	0 g 0 LSB	1 g 4096 LSB	-1 g -4096 LSB

3 Hardware Interface Description and Packaging

3.1 Package Parameters

Parameter	Value	Unit
Width	2.0	mm
Length	2.0	mm
Height	0.95	mm
Weight	8.65	mg

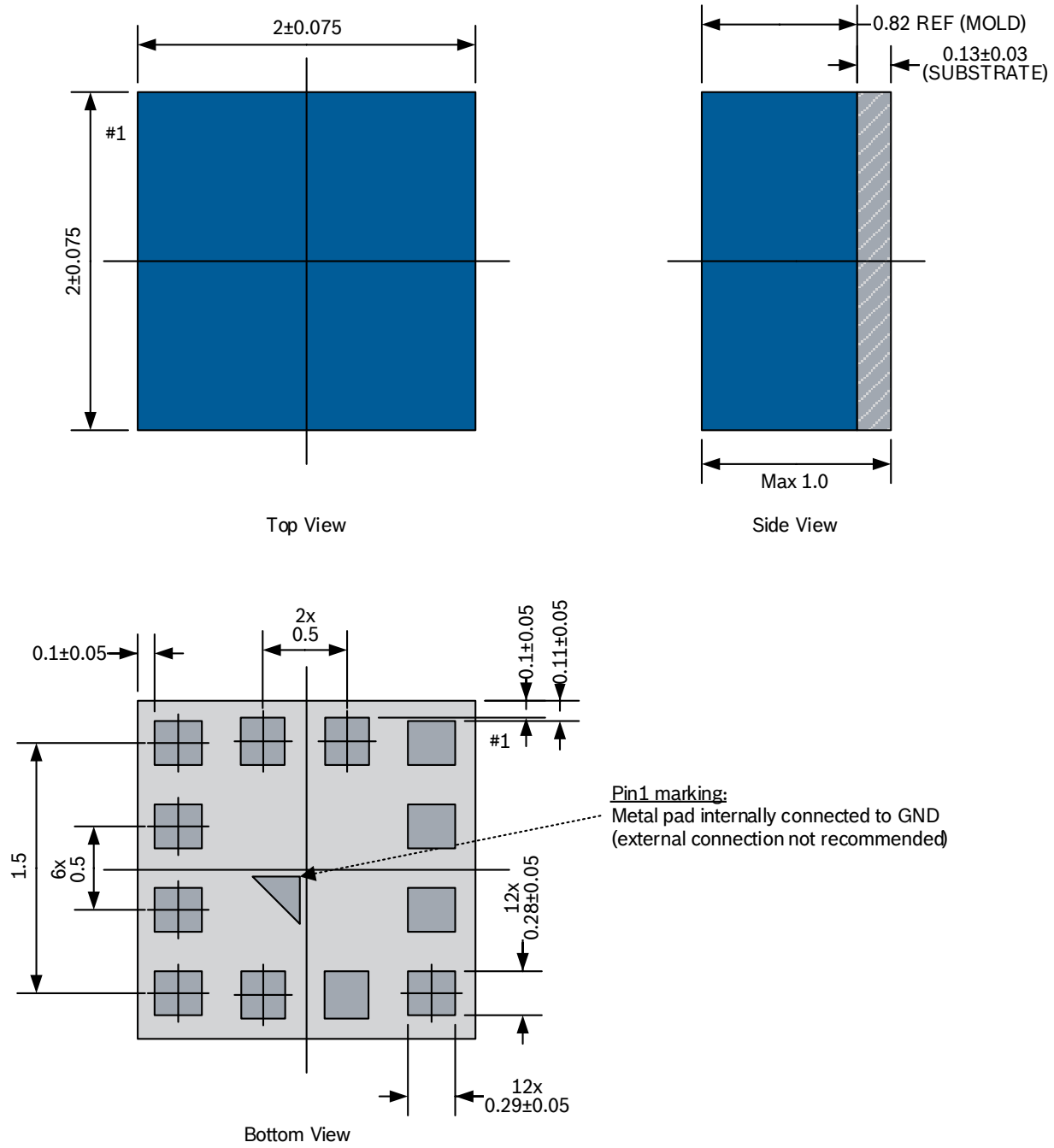


Figure 6 SMA131 package outline drawing

The dimensions are given in mm. Note: Unless otherwise specified, the tolerance is ± 0.05 mm.

The sensor housing is a standard LGA package.

3.2 Transport Package

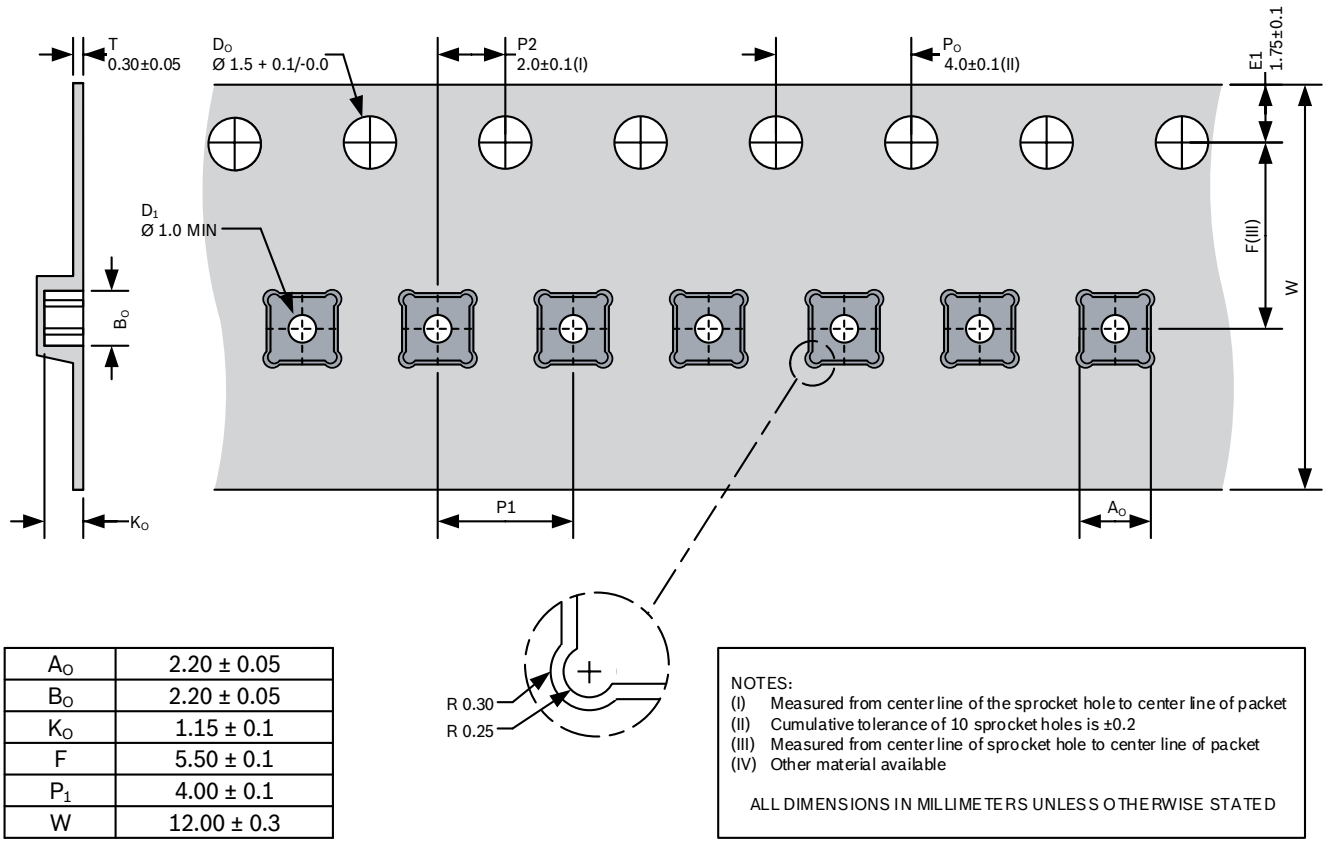
3.2.1 Tape on Reel Specification

The SMA131 is shipped in a standard cardboard box.

The box dimensions for one reel are L x W x H = 35 cm x 35 cm x 6 cm.

SMA131 quantity: 10000 pcs per reel. Please handle with care.

3.2.2 Tape Dimensions



A_O	2.20 ± 0.05
B_O	2.20 ± 0.05
K_O	1.15 ± 0.1
F	5.50 ± 0.1
P_1	4.00 ± 0.1
W	12.00 ± 0.3

NOTES:
(I) Measured from center line of the sprocket hole to center line of packet
(II) Cumulative tolerance of 10 sprocket holes is ±0.2
(III) Measured from center line of sprocket hole to center line of packet
(IV) Other material available

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED

Figure 7 Tape dimensions in mm

3.2.3 Reel Dimensions

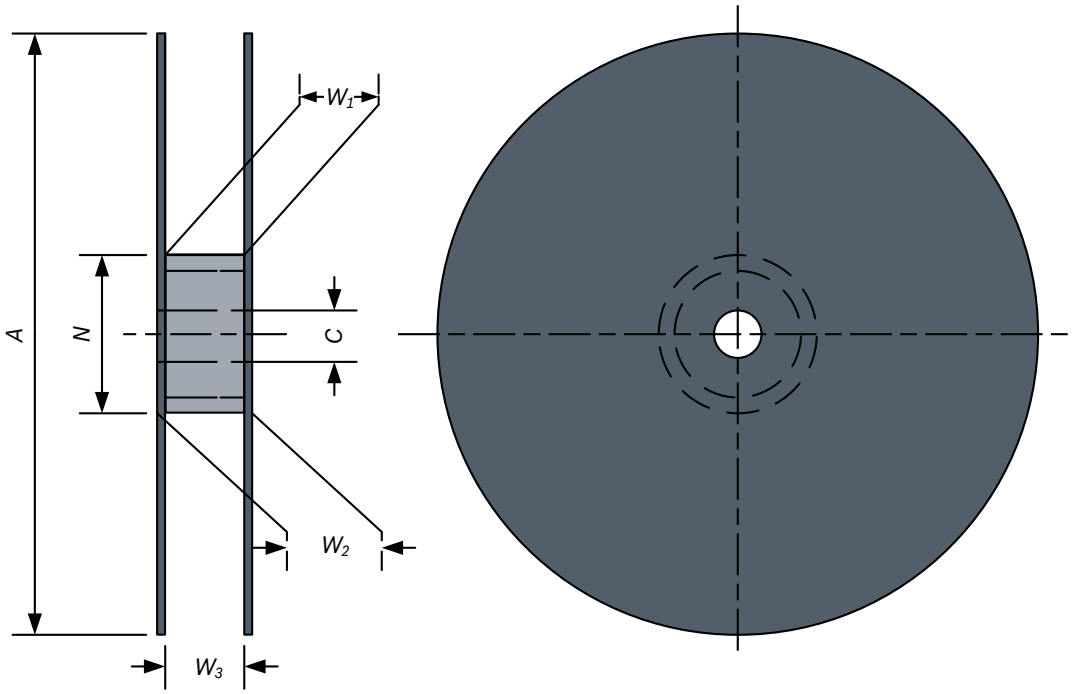


Figure 8 Reel dimension

Parameter	Meaning	Dimensions [mm]
W (not depicted)	tape width	12
A	reel diameter	330
N	hub diameter	100
W_1	inner width of reel	12.4 +2
W_2	total width of reel	18.4
W_3, min	inner width of reel, minimum	11.9
W_3, max	inner width of reel, maximum	15.4

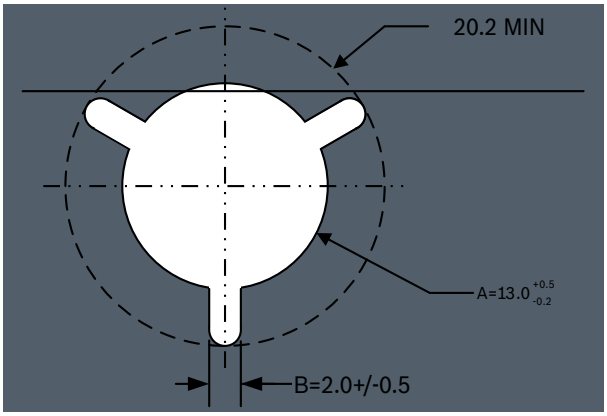


Figure 9 Details on hub hole dimension C in mm

3.2.4 Orientation within the Reel

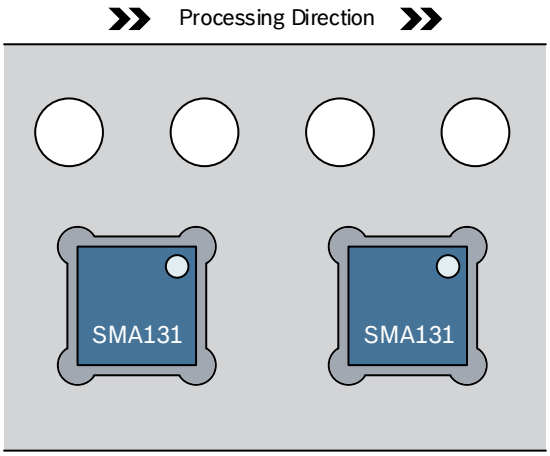


Figure 10 Orientation of the SMA131 devices relative to the tape

3.3 Labeling of the Product

Labeling	Name	Symbol	Remark
	Counter ID	CCC	3 alphanumeric digits, variable to generate trace-code
	Type ID	V	1 character to identify product type for the SMA131, this character is fixed as “V”
	Subcon ID	A	1 alphanumeric digit to identify subcon for the SMA131, this digit is fixed as “A”
	Pin 1 identifier	●	--

3.4 Pinning

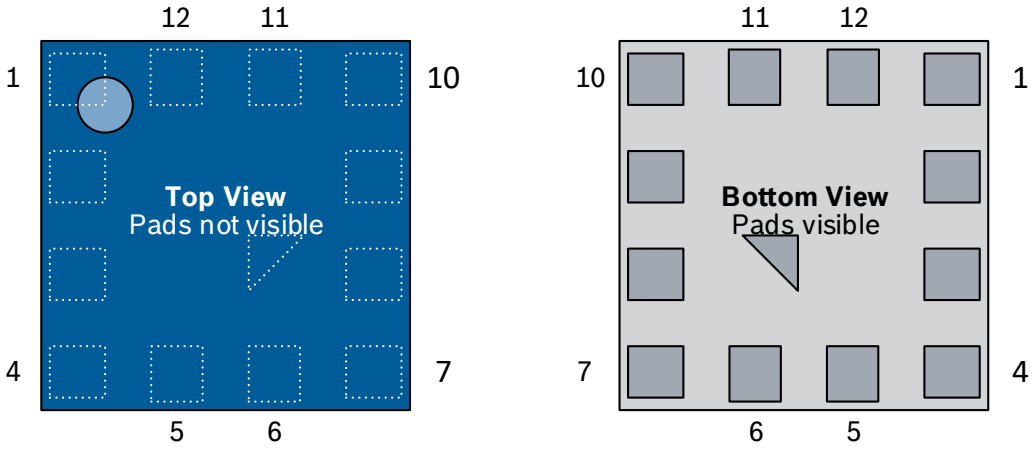


Figure 11 Pin-out top view (left) and bottom view (right)

Pin	Name	I/O Type	Description	Connect to - SPI -	Connect to - TWI -
1	SDO	Digital out	SPI: serial data out TWI: address select	SDO	GND for default address
2	SDx	Digital I/O	SPI: SDI (serial data in) TWI: SDA (serial data I/O)	SDI	SDA
3	VDDIO	Supply	Digital I/O supply voltage	VDDIO	VDDIO
4	NC	-	-	GND	GND
5	INT1	Digital out	Interrupt pin 1	INT1 / DNC	INT1 / DNC
6	NF	-	-	DNC	DNC
7	VDD	Supply	Power supply analog & digital domain	VDD	VDD
8	GNDIO	Ground	Ground for I/O	GND	GND
9	GND	Ground	Ground for analog & digital domain	GND	GND
10	CSB	Digital in	SPI: chip select TWI: DNC	CSB	DNC (float)
11	PS	Digital in	Protocol select	GND	VDDIO
12	SCx	Digital in	Serial clock	SCK	SCL

NC: Not connected
NF: No function
DNC: Do not connect
INT1: If not needed, DNC

3.5 Soldering

The moisture sensitivity level (MSL) of BOSCH SMA131 corresponds to JEDEC Level 1, see also

- IPC/JEDEC J-STD-020C “Joint Industry Standard: Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices”
- IPC/JEDEC J-STD-033A “Joint Industry Standard: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitivity Surface Mount Devices”

The sensor IC fulfils the lead-free soldering requirements of the above-mentioned IPC/JEDEC standard, i.e., reflow soldering with a peak temperature up to 260°C. Repair and manual soldering of the sensor is not permitted.

3.5.1 Reflow Soldering Recommendation for Sensors in LGA Package

Please make sure that the edges of the LGA substrate of the sensor are free of solder material. Avoid solder material forming a high meniscus covering the edge of the LGA substrate (see Figure 12).

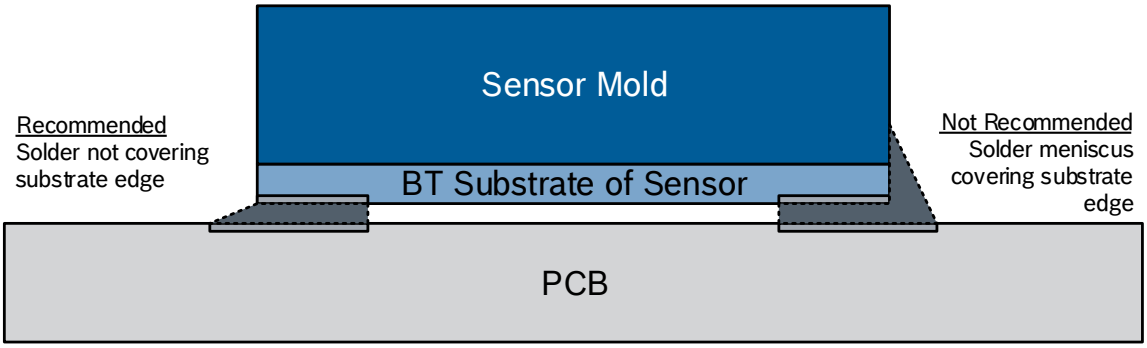


Figure 12 Reflow soldering recommendation

3.5.2 Classification Reflow Profiles

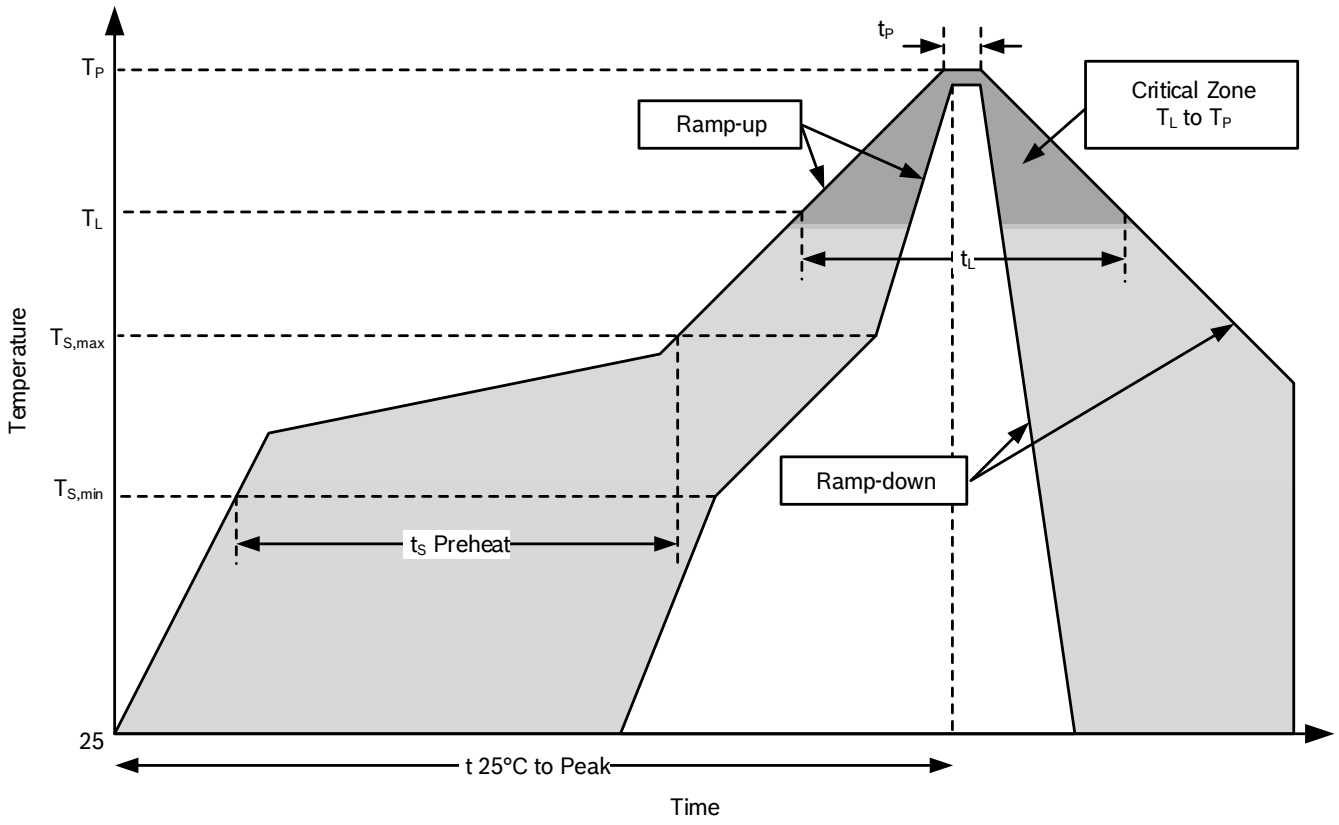


Figure 13 Soldering profile

Profile Feature	Pb-Free Assembly
Average ramp-up rate (Ts_{max} to Tp)	3 °C/s max.
Preheat Temperature min (Ts_{min}) Temperature max (Ts_{max}) Time (ts_{min} to ts_{max})	 150 °C 200 °C 60 s – 80 s
Time maintained above: Temperature (T_L) Time (t_L)	 217 °C 60 s – 150 s
Peak classification temperature (Tp)	260 °C
Time within 5 °C of actual peak	20 s – 40 s
Ramp-down rate	6 °C/s max.
Time 25 °C to peak temperature	8 min max.

Note: All temperatures refer to the topside of the package, measured on the package body surface.

3.5.3 Multiple Reflow Soldering Cycles

The product can withstand up to 3 reflow soldering cycles in total. This could be a situation where a PCB is mounted with devices from both sides (i.e. 2 reflow cycles necessary) or where, in the next step, an additional re-work cycle could be required (1 reflow).

3.6 Mounting Recommendations

MEMS sensors in general are high-precision measurement devices which consist of electronic as well as mechanical structures. BOSCH sensor devices are designed for precision, efficiency and mechanical robustness.

However, in order to achieve best possible results of your design, the following recommendations should be taken into consideration when mounting the sensor on a printed circuit board (PCB).

In order to evaluate and optimize the considered placement position of the sensor on the PCB it is recommended to use additional tools during the design in phase, e.g.:

- Regarding thermal aspects: infrared camera
- Regarding mechanical stress: warpage measurements and/or FEM-simulations
- Regarding shock robustness: drop test of the devices after soldering on the target application PCB

Recommendations in Detail

- It is recommended to keep a reasonable distance between the sensor mounting location on the PCB and the critical points described in the following examples. The exact value for a “reasonable distance” depends on many customer specific variables and must therefore be determined case by case.
- It is not recommended to place the sensor directly under or next to push-button contacts as this can result in mechanical stress.
- It is not recommended to place the sensor in direct vicinity of extremely hot spots regarding temperature (e.g. a µController or a graphic chip) as this can result in heating up the PCB and consequently also the sensor.
- It is not recommended to place the sensor in direct vicinity of a mechanical stress maximum (e.g. in the center of a diagonal crossover). Mechanical stress can lead to bending of the PCB and the sensor.
- Do not mount the sensor too closely to a PCB anchor point where the PCB is attached to a shelf (or similar) as this could also result in mechanical stress. To reduce potential mechanical stress, minimize redundant anchor points and/or loosen respective screws.
- Avoid mounting the sensor in areas where resonant amplitudes (vibrations) of the PCB are likely or to be expected.
- Please avoid partial coverage of the sensor by any kind of (epoxy) resin, as this can possibly result in mechanical stress.
- Avoid mounting (and operation) of the sensor in the vicinity of strong magnetic, strong electric and/or strong infrared radiation fields (IR).
- Avoid electrostatic charging of the sensor and of the device in which the sensor is mounted.

In case you have any questions regarding the mounting of the sensor on your PCB or the evaluation and/or optimization of the considered placement position of the sensor on your PCB, do not hesitate to contact us.

If the above mentioned recommendations cannot be realized appropriately, a specific in-line offset calibration after placement of the device onto your PCB might help to minimize potentially remaining effects.

The SMA131 is designed to sense accelerations with high accuracy even at low amplitudes and contains highly sensitive structures inside the sensor element. The MEMS sensor can tolerate mechanical shocks up to several thousand g’s. However, these limits might be exceeded in conditions with extreme shock loads such as e.g. hammer blow on or next to the sensor, dropping the sensor onto hard surfaces etc.

We strongly recommend to avoid any g forces beyond the limits specified in the data sheet during transport, handling and mounting of the sensors in a defined and qualified installation process.

This device has built-in protections against high electrostatic discharges or electric fields (2 kV HBM). However, anti-static precautions should be taken as for any other CMOS component.

Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be connected to a defined logic voltage level.

3.7 Recommendations for PCB Layout

For the design of the landing patterns, the dimensioning as shown in Figure 14 is recommended. The dimensions are given in mm.

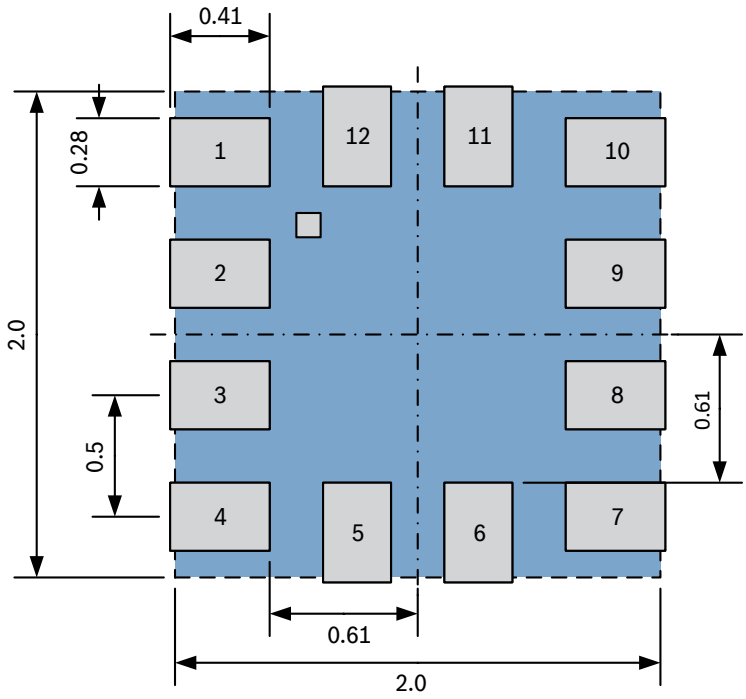


Figure 14 SMA131 footprint. All dimensions are given in mm

The same tolerances as given for the outline dimensions (Figure 6) should be assumed.

A wiring no-go area in the top layer of the PCB below the sensor is strongly recommended (e.g. no vias, wires or other metal structures).

4 Environment Specification

4.1 Absolute Maximum Ratings

Any values beyond the given ratings may seriously damage the device. The sensor must be discarded when exceeding these limits.

Parameter	Condition	Min	Max	Unit
Voltage at supply pin	VDD pin	-0.3	4.25	V
Voltage at supply pin	VDDIO pin	-0.3	4.25	V
Voltage at any logic pin	Non-supply pin	-0.3	VDDIO + 0.3	V
Mechanical shock	Free fall onto hard surfaces		1.8	m
Mechanical shock	Duration ≤ 1 ms		2000	g
ESD	HBM, at any pin		2	kV
ESD	CDM		500	V
ESD	MM		200	V

4.2 Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating temperature	T	-40	-	85	°C
Extended operating temperature (details see chapter 5.2.2)	$T_{extended}$	-40	-	105	°C

4.3 Lifetime Conditions

Parameter	Condition
Lifetime	according to AEC-Q100 grade 3 requirements

4.4 Environmental Safety

RoHS

The SMA131 sensor meets the requirements of the *Restriction of Hazardous Substances* (RoHS) directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 (on the *Restriction of the use of certain Hazardous Substances in electrical and electronic equipment)*.

The sensor module is recyclable according to the norm WEEE - 2012/19/EU.

Halogen content

The SMA131 is halogen-free. For more details on the analysis results, please contact your Bosch representative.

5 Parameter Specification

5.1 Power Supply

The SMA131 has two distinct power supply pins:

- VDD is the main power supply for the internal blocks.
- VDDIO is a separate power supply pin mainly used for the supply of the interface.

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Supply voltage internal domains	VDD		1.62	2.4	3.6	V
Supply voltage I/O domain	VDDIO		1.2	2.4	3.6	V
Voltage input low level	V_{IL}				0.3 VDDIO	-
Voltage input high level	V_{IH}		0.7 VDDIO			-
Voltage output low level	V_{OL}	I_{OL} = 3 mA			0.2 VDDIO	-
Voltage output high level	V_{OH}	I_{OH} = 3 mA, SPI	0.8 VDDIO			-

There are no limitations regarding the voltage levels of both pins relative to each other as long as each of them is within the specified operating range. Furthermore, the device can be completely switched off (VDD = 0 V) while keeping the VDDIO supply on (VDDIO > 0 V) or vice versa.

In the case that the VDDIO supply is switched off, all interface pins (CSB, SDI, SCK, PS) must be kept close to GNDIO potential.

The SMA131 provides a **power-on reset (POR)** generator. It resets the logic part and the register values after powering on VDD and VDDIO. After POR, all settings are reset to the default values. All application specific settings which are not equal to the default settings have to be reset to their designated values after POR.

There are no constraints on the switching sequence of VDD and VDDIO. In the case that the TWI interface be used, a direct electrical connection between VDDIO and the PS pin is needed in order to ensure reliable protocol selection. For SPI mode, the PS pin must be directly connected to GNDIO.

5.2 Technical Data

The data in this chapter, unless otherwise noted, apply for the valid operation conditions given in section 4.2 and 19. All following figures include voltage, temperature and lifetime effects if not noted otherwise. All figures except for sensitivity are only valid without an external stimulus being applied. All operation conditions are only valid if no failure flags indicate any malfunction. All figures except for the noise itself exclude noise effects.

The sensor was validated and qualified in the temperature range from -40 °C to 85 °C according to Bosch standard release process. Within this temperature range the values in the TCD section 5.2.1 were specified.

For the values between 85 °C and 105 °C a characterization over the full temperature range (-40 °C to 105 °C) was performed without consideration of lifetime effects, however the sensor will not be destroyed through thermal event in this temperature range. Within this temperature range, the values in section 5.2.2 are valid. It is the customers' responsibility to assess the impact on system level.

Parameter	Symbol	Comment	Range (typical)	Unit	Resolution (typ., 25°C)	Unit
Measurement range | Resolution	g_{FS}	selectable	±2 ±4 ±8	g	4096 2048 1024	LSB/g
Bandwidth	BW	Selectable 2nd order filter	8, 16, 31, 63, 125, 250, 500			Hz

5.2.1 Values in the Temperature Range -40 °C to 85 °C

Unless otherwise specified, the sensor is configured with the default settings. The measurement range is set to 2 g and the bandwidth is set to 1000 Hz.

Parameter	Symbol	Condition / Comment	Typical	Max[1]	Unit
Total supply current in normal mode	I_{DD}	T = 25 °C, ODR_{max}, VDD = VDDIO = 2.4 V	130		µA
Total supply current in suspend mode	I_{DDsum}	T = 25 °C, VDD = VDDIO = 2.4 V	1.4		µA
Total supply current in deep suspend mode	I_{DDdsum}	T = 25 °C, VDD = VDDIO = 2.4 V	1.0		µA
Total supply current in low power mode 1	I_{DDlp1}	T = 25 °C, unfiltered, VDD = VDDIO = 2.4 V, sleep duration = 25 ms	6.9		µA
Start-up time	$t_{s,up}$	POR, ODR_{max}	1.2		ms
Wake-up time 1	$t_{w,up1}$	from low power mode 1, suspend mode or deep suspend mode, ODR_{max}	1.4		ms
Sensitivity tolerance		including temperature, axis and lifetime effects		±5.0	%
Temperature Coefficient Sensitivity	TCS	nominal VDD supply, over full temperature range, no lifetime	0.014		%/K
Zero-g Offset		including temperature, axis and lifetime effects		±150	mg
Zero-g Offset		T = 25 °C over lifetime	±45		mg
Temperature Coefficient Offset (zero-g)	TCO	nominal VDD supply, over full temperature range, no lifetime	±0.7		mg/K

[1] For specified maximum values, please refer to the Technical Customer Documentation

Output data rate	ODR_{max}	unfiltered	2000	Hz
Nonlinearity	NLIN	best fit straight line, no life-time, T = 25 °C	±2.5	% FS
Noise rms		T = 25 °C, BW = 1000 Hz, including axis and lifetime effects	3.9	mg
Noise rms		T = 25 °C, BW = 31.25 Hz, no lifetime	0.9	mg
Cross axis sensitivity		T = 25 °C, no lifetime	1	%
Alignment error		MEMS element relative to package outline		°

5.2.2 Values in the Temperature Range 85 °C to 105 °C

Parameter	Symbol	Condition / Comment	Typical	Unit
Sensitivity tolerance		over full temperature range, w/o lifetime effects	±2.1	%
Temperature Coefficient Sensitivity	TCS	nominal VDD supply, over full temperature range, w/o lifetime effects	0.014	%/K
Zero-g offset		over full temperature range, w/o lifetime effects	±70	mg
Temperature Coefficient Offset (zero-g)	TCO	nominal VDD supply, over full temperature range, w/o lifetime effects	±0.7	mg/K
Nonlinearity	NLIN	over full temperature range, w/o lifetime effects	±2.5	% FS
Noise rms		nominal VDD supply, over full temperature range, w/o lifetime effects, BW = 1000 Hz	5.2	mg
Noise rms		nominal VDD supply, over full temperature range, w/o lifetime effects, BW = 31.25 Hz	1.1	mg

6 Software Interface Description

The SMA131 supports two serial digital interface protocols for communication as a slave with a host device, SPI and I²C compatible TWI. The active interface is selected by the state of the protocol select (PS) pin: 0 (1) selects SPI (TWI).

Both interfaces share the same pins. The mapping for each interface is given in the table below.

Pin	Name	Use with SPI	Use with TWI	Description
1	SDO	SDO	Address	SPI: serial data output TWI: used to set LSB of TWI address
2	SDx	SDI	SDA	SPI: serial data input TWI: serial data
10	CSB	CSB	Unused	SPI: chip select (enable) TWI: do not connect
12	SCx	SCK	SCL	Serial clock

The electrical specifications of the interface pins are shown in the table below.

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Pull-up resistance, CSB pin	R_{up}	Internal pull-up resistance to VDDIO	75	100	125	kΩ
Input capacitance	C_{in}			5	10	pF
TWI bus load capacitance (max. drive capability)	C_{TWI_load}				400	pF

6.1 Serial Peripheral Interface (SPI)

6.1.1 SPI Connection

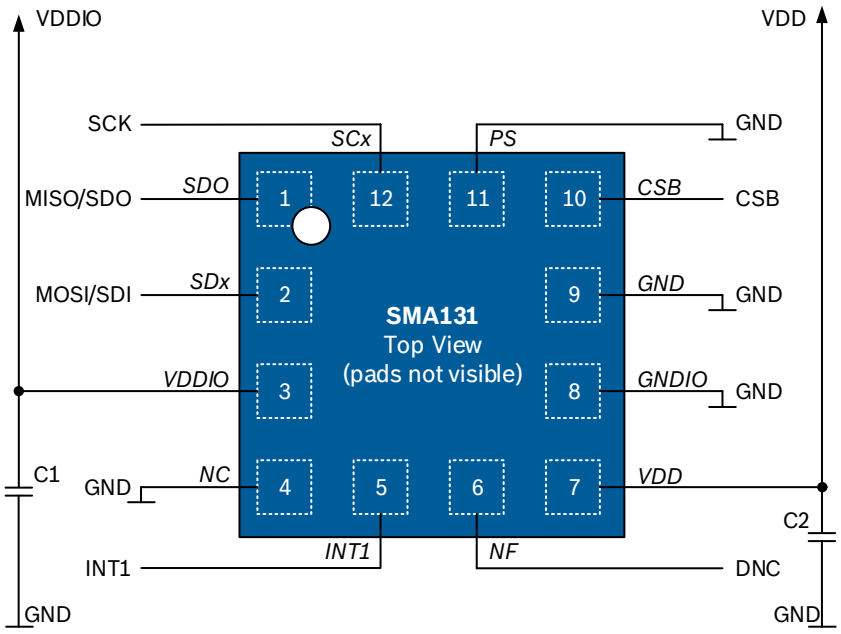


Figure 15 SPI connection diagram

C_1, C_2: 100 nF
INT: see register

Note:

For a proper functionality defined voltage levels at SDI, SDO and SCK are required. In case this cannot be guaranteed by the SPI controller, additional pull-up or pull-down resistors are required.

6.1.2 SPI Timing

The timing specification for SPI of the SMA131 is given in the table below.

Parameter	Symbol	Condition	Min	Max	Unit
Clock frequency	f_{SPI}	max. load on SDI or SDO = 25 pF, VDDIO ≥ 1.62 V		10	MHz
Clock frequency	f_{SPI}	max. load on SDI or SDO = 25 pF, VDDIO < 1.62 V		7.5	MHz
SCK low pulse	t_{SCKL}		20		ns
SCK high pulse	t_{SCKH}		20		ns
SDI setup time	t_{SDI_setup}		20		ns
SDI hold time	t_{SDI_hold}		20		ns
SDO output delay	t_{SDO_OD}	load = 25 pF, VDDIO ≥ 1.62 V		30	ns
SDO output delay	t_{SDO_OD}	load = 25 pF, VDDIO < 1.62 V		50	ns
SDO output delay	t_{SDO_OD}	load = 250 pF, VDDIO > 2.4 V		40	ns
CSB setup time	t_{CSB_setup}		20		ns
CSB hold time	t_{CSB_hold}		40		ns
Idle time between write accesses in normal mode	$t_{IDLE\_wacc\_nm}$		2		µs
Idle time between write accesses, suspend mode, low power mode 1	$t_{IDLE\_wacc\_sum}$		450		µs

Figure 16 shows the definition of the SPI timings.

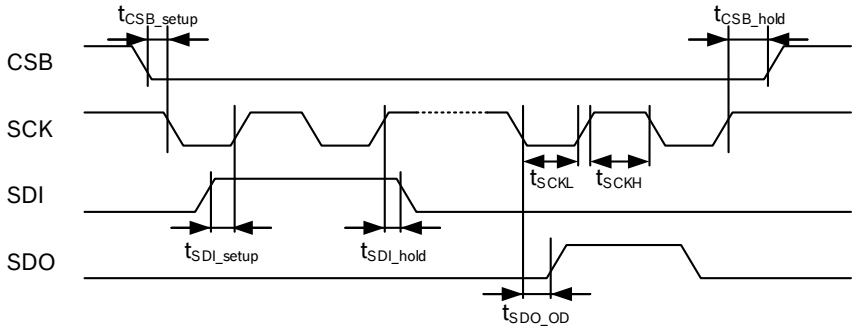


Figure 16 SPI timing diagram

The SPI interface of the SMA131 is compatible with two modes, 00 and 11. The automatic selection between [CPOL = 0 and CPHA = 0] and [CPOL = 1 and CPHA = 1] is controlled based on the value of SCK after a falling edge of CSB. For single byte read as well as write operations, 16-bit protocols are used. The SMA131 also supports multiple-byte read operations.

For the standard SPI configuration, CSB (chip select low active), SCK (serial clock), SDI (serial data input) and SDO (serial data output) pins are used. The communication starts when CSB is pulled low by the SPI

master and stops when CSB is pulled high. SCK is also controlled by the SPI master. SDI and SDO are driven at the falling edge of SCK and should be captured at the rising edge of SCK.

The basic write operation waveform for SPI configuration is depicted in Figure 17. During the full write cycle, SDO remains in high-impedance state.

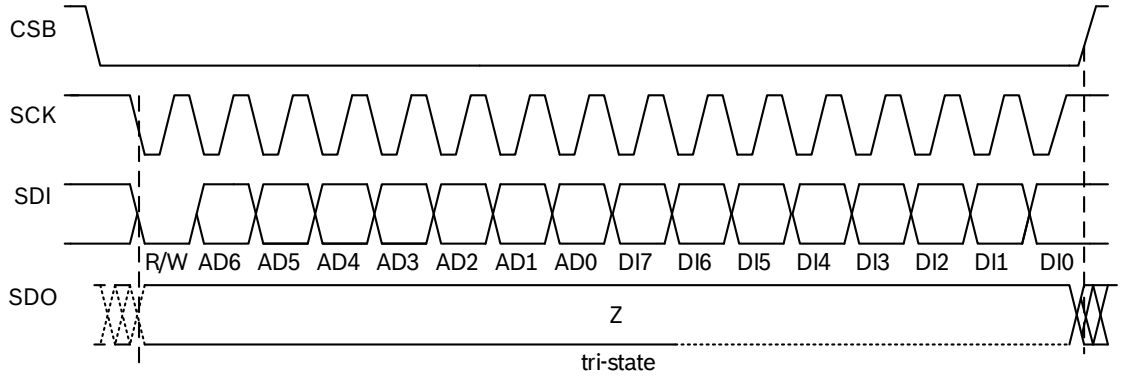


Figure 17 Basic SPI write sequence (mode11)

The basic read operation waveform for SPI configuration is depicted in Figure 18.

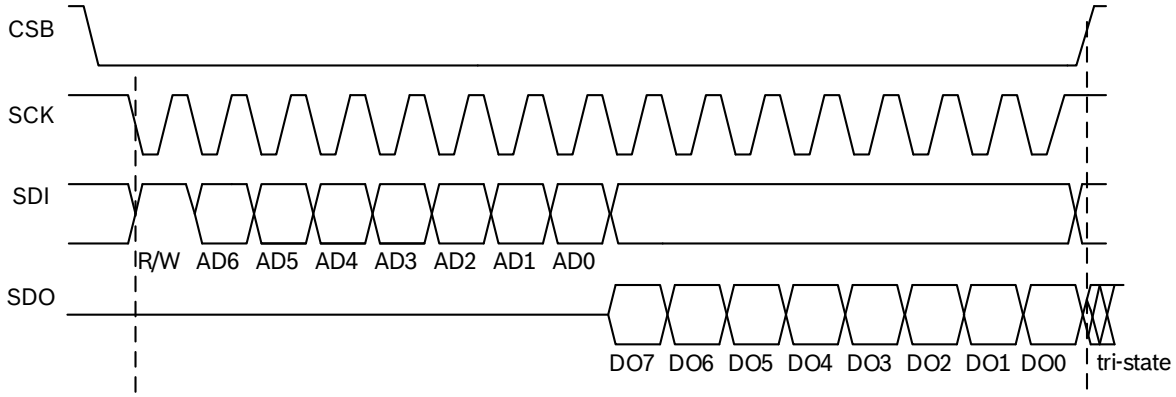


Figure 18 Basic SPI read sequence (mode 11)

The data bits are used as follows:

Bit <15>: Read/write bit. When 0, the data SDI is written into the chip. When 1, the data SDO from the chip is read.

Bits <14:8>: Address AD (6:0)

Bits <7:0>: When in write mode, these bits are the data SDI which will be written into the address. When in read mode, these bits are the data SDO which are read from the address.

Multiple read operations are possible by keeping CSB low and continuing the data transfer. Only the first register address has to be written. Addresses are automatically incremented after each read access as long as CSB stays active low.

The principle of a multiple read operation is shown in Figure 19.

	Control Byte								Data Byte								Data Byte								Data Byte								
Start	RW	Register Address (02h)							Data Register – Address 02h								Data Register – Address 03h								Data Register – Address 04h								Stop
CSB = 0	1	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CSB = 1

Figure 19 SPI multiple read

6.2 Two-wire Interface (TWI)

With some exceptions, the TWI interface of the SMA131 is compatible to the I²C specification UM10204 Rev. 03 (19 June 2007), available at http://www.nxp.com.

- The SMA131 supports the I²C standard and fast mode, but only the 7-bit address mode.
- For VDDIO = 1.2 ... 1.8 V the granted voltage output levels are slightly relaxed compared to the specification.
- The internal data hold time (t_{HDDAT}) of 300 ns is not met under all operation conditions. The device achieves a minimum value of 120 ns across process corners and temperature.
- The minimum data fall time (t_F) of ≥ 20 ns cannot be met.
- Only single byte write is supported.
- Detection of a stop condition is not supported. All data transfer protocols are fully operational by means of detecting the start condition only.
- The device does not support the high-impedance mode while VDDIO is tied to GND.
- The device does not perform clock stretching, i.e., clock frequencies may not exceed the one specified in the parameter section, and wait times between subsequent write accesses (as specified in section 6.2.2) have to be ensured by the bus master.

6.2.1 TWI Connection

The TWI bus uses SCL (= SCx pin, serial clock) and SDA (= SDx pin, serial data input and output) signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free.

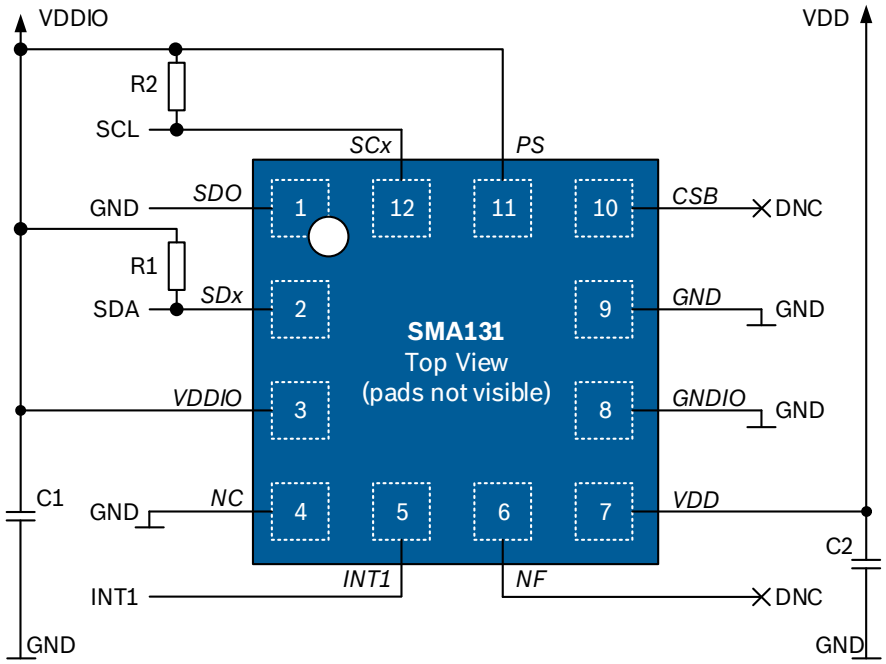


Figure 20 TWI connection diagram

C_1, C_2: 100 nF
R_1, R_2: pull-up resistors

The default TWI address of the SMA131 is 0x18 (0011000). It is used if the SDO pin is pulled to GND. The alternative address 0x19 (0011001) is selected by pulling the SDO pin to VDDIO.

6.2.2 TWI Timing

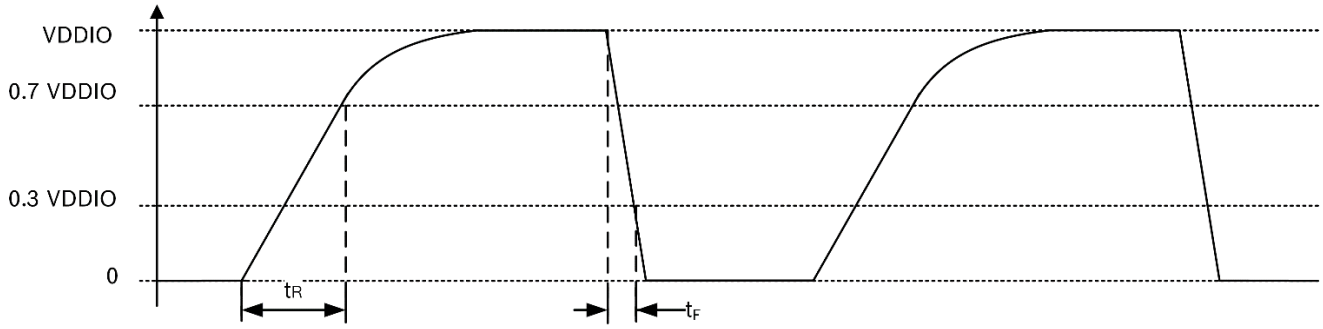


Figure 21 Definition of rise and fall time of TWI signals

The TWI timing specification for the SMA131 is given in the table below.

Parameter	Symbol	Min	Max	Unit
Clock frequency	f_{SCL}		400	kHz
SCL low period	t_{LOW}	1.3		µs
SCL high period	t_{HIGH}	0.6		µs
SDA setup time	t_{SUDAT}	0.1		µs
SDA hold time	t_{HDDAT}	0.0		µs
Setup time for a repeated start condition	t_{SUSTA}	0.6		µs
Hold time for a start condition	t_{HDSTA}	0.6		µs
Setup time for a stop condition	t_{SUSTO}	0.6		µs
Time before a new transmission can start	t_{BUF}	1.3		µs
Idle time between write accesses in normal mode	$t_{IDLE\_wacc\_nm}$	2		µs
Idle time between write accesses, suspend mode, low power mode 1	$t_{IDLE\_wacc\_sum}$	450		µs

Figure 22 shows the definition of the TWI timing given in the table above.

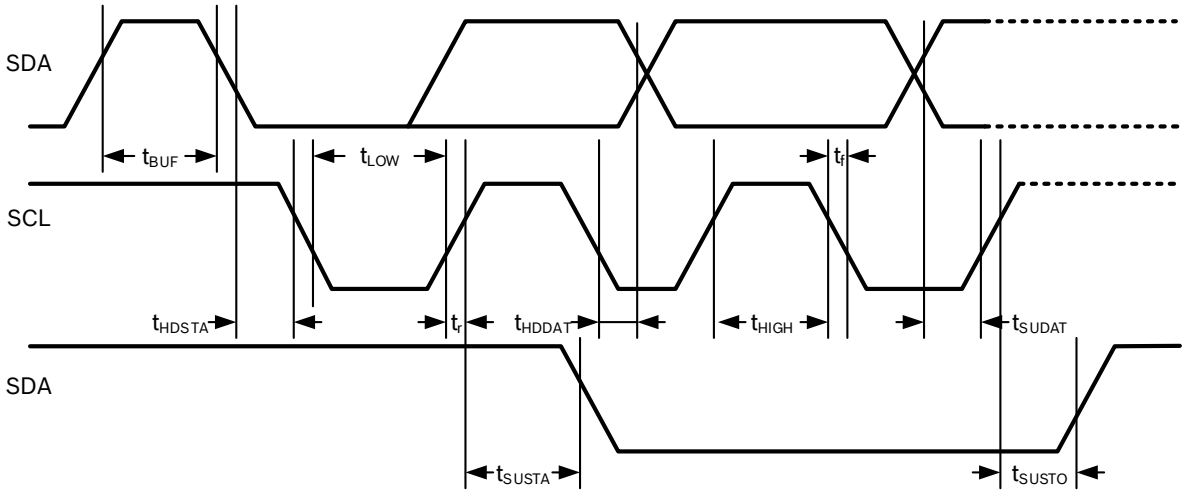


Figure 22 SMA131 TWI timing specification

The TWI protocol works as follows:

Mode	Description
START:	Data transmission on the bus begins with a high to low transition on the SDA line while SCL is held high (start condition (S) indicated by the TWI bus master). Once the start signal is transferred by the master, the bus is considered busy.
STOP:	Each data transfer should be terminated by a stop signal (P) generated by the master. The stop condition is a low to high transition on the SDA line while SCL is held high.
ACK:	Each byte of data transferred must be acknowledged. It is indicated by an acknowledge bit sent by the receiver. The transmitter must release the SDA line (no pull down) during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.

In the following diagrams these abbreviations are used:

S	Start	**P**	Stop
ACKS	Acknowledge by slave	**ACKM**	Acknowledge by master
NACKM	Not acknowledge by master	**RW**	Read / Write

A start (S) immediately followed by a stop (P) (without SCK toggling from VDDIO to GND) is not supported and not recognized by the SMA131.

TWI write access can be used to write a data byte in one sequence.

The sequence begins with a start condition generated by the master, followed by 7 bits of slave address and a write bit (RW = 0). The slave sends an acknowledge bit (ACK = 0) and releases the bus. Then the master sends the one byte register address. The slave again acknowledges the transmission and waits for the 8 bits of data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol. Figure 23 shows an example of a TWI write access.

									Control Byte									Data Byte									
Start	Slave Address							RW	ACKS	Register Address (0x10)								ACKS	Data (0x09)								ACKS	Stop
S	0	0	1	1	0	0	0	0		0	0	0	1	0	0	0	0		X	X	X	X	X	X	X	X		P

Figure 23 TWI write access

TWI read access can be used to read one or multiple data bytes in one sequence.

A read sequence consists of a one-byte TWI write phase followed by the TWI read phase. Both parts of the transmission must be separated by a repeated start condition (Sr). The TWI write phase addresses the slave and sends the register address to be read. After the slave acknowledges the transmission, the master again generates a start condition and sends the slave address together with a read bit (RW = 1). Then the master releases the bus and waits for the data bytes to be read out from the slave. After each data byte the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACKM (ACK = 1) from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a stop condition and terminate the transmission.

The register address is automatically incremented. Hence, more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified in the latest TWI write command. By default the start address is set as 0x00. In this way, repetitive multi-byte reads from the same starting address are possible.

In order to prevent the TWI slave from locking up the TWI bus, a watchdog timer (WDT) is implemented. The WDT observes internal TWI signals and resets the TWI interface if the bus is locked up. Activity and timer period of the WDT can be configured via bits 2 (*i2c_wdt_en*) and 1 (*i2c_wdt_sel*) in register 0x34 (BGW_ WDT).

- Writing 1 (0) to *i2c_wdt_en* activates (de-activates) the WDT.
- Writing 0 (1) to *i2c_wdt_sel* selects a timer period of 1 ms (50 ms).

Figure 24 shows an example of a TWI multiple read access.

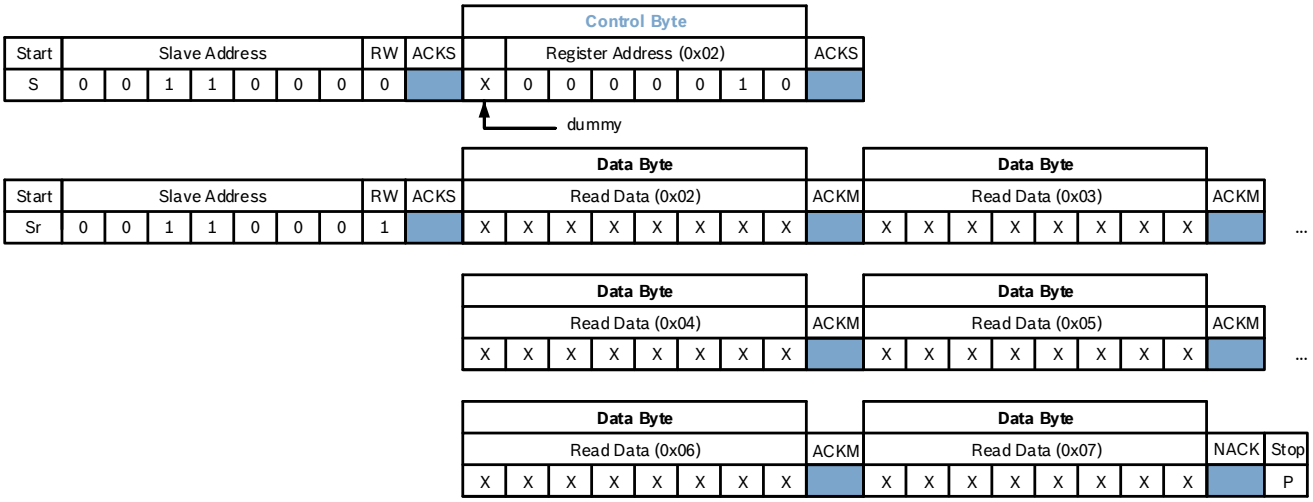


Figure 24 TWI multiple read access

6.3 Access Restrictions (SPI and TWI)

In order to allow for the correct internal synchronization of data written to the SMA131, certain access restrictions apply for consecutive write accesses or a write/read sequence through the SPI and TWI interface. The required waiting period depends on whether the device is operating in normal mode or suspend mode (also low power mode 1).

As illustrated in Figure 25, an interface idle time of at least 2 µs is required following a write operation when the device operates in normal mode. In suspend mode (also low power mode 1), an interface idle time of at least 450 µs is required.

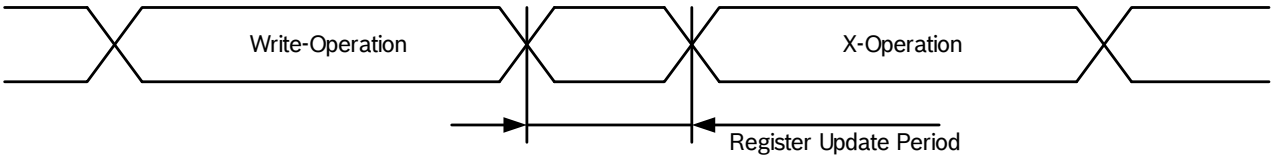


Figure 25 Post-write access timing constraints

7 Application Details

In Figure 26 the basic flow chart for the sensor application is shown. Three different categories of functional elements are shown:

- Required: these blocks are mandatory for a proper sensor functionality and retrieving data (e.g. read data)
- Recommended: these blocks are useful to detect potential sensor failure and to allow further configuration of the sensor (e.g. self-test, sensor setup)
- Optional: depending on the customer specific application, these blocks might be required (e.g. interrupt configuration)

The functional elements are described in the following sections. Proper function of the sensor in the overall system must be validated by the customer.

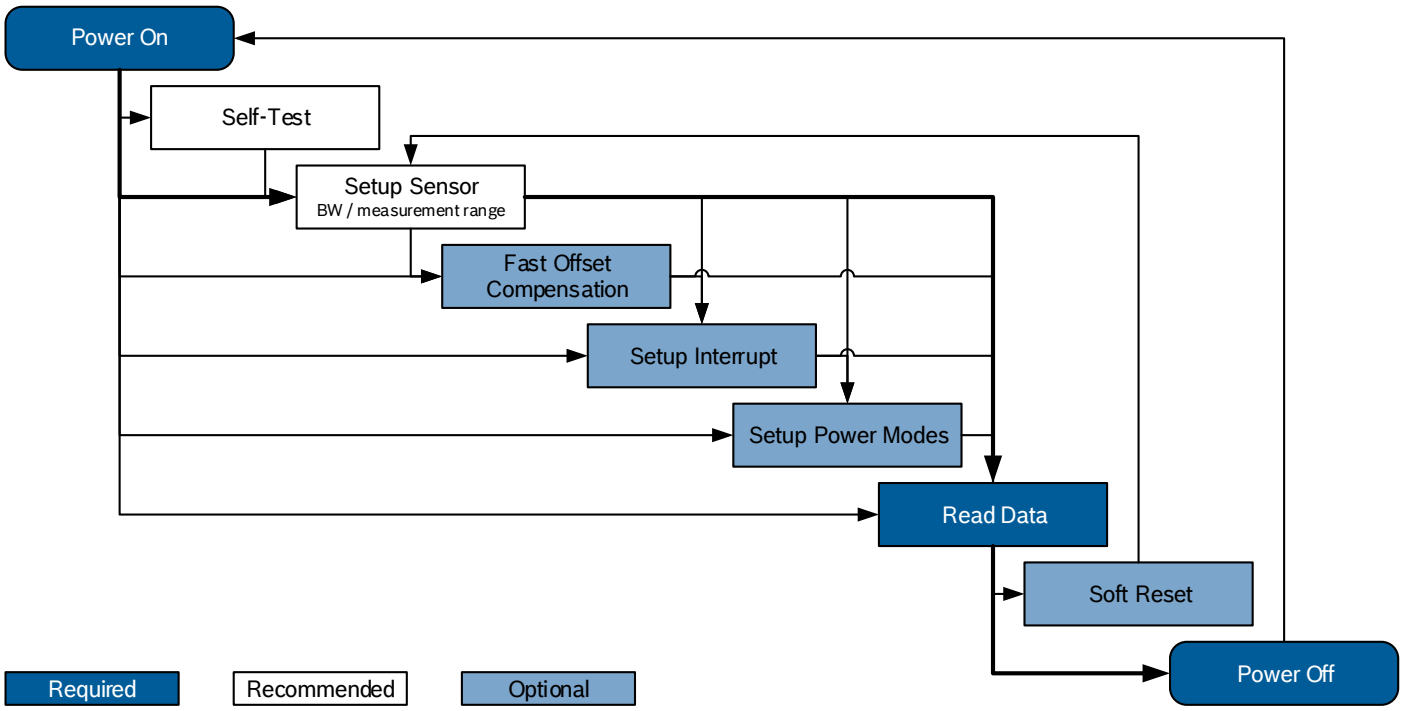


Figure 26 Basic flow chart for SMA131 application with key functional elements

7.1 Sensor Settings

The **bandwidth** of filtered acceleration data is determined by setting bits <4:0> (*bw*) in register 0x10 (PMU_BW) as shown in the following table.

bw <4:0>	Bandwidth	Update Time
00xxx	*)	-
01000	7.81 Hz	64 ms
01001	15.63 Hz	32 ms
01010	31.25 Hz	16 ms
01011	62.5 Hz	8 ms
01100	125 Hz	4 ms
01101	250 Hz	2 ms
01110	500 Hz	1 ms
01111	1000 Hz	0.5 ms
1xxxx	*)	-

*) The *bw* settings 00xxx and 1xxxx are both reserved. *bw* = 00xxx results in a bandwidth of 7.81 Hz, *bw* = 1xxxx results in an unfiltered signal. It is recommended to actively set an appropriate, application specific bandwidth and to use the *bw* range from 01000 to 01111.

The acceleration measurement **range** can be selected via bits <3:0> (*range*) in register 0x0F (PMU_RANGE) according to the table below.

range <3:0>	Measurement Range	Resolution
0011	±2 g	4096 LSB/g
0101	±4 g	2048 LSB/g
1000	±8 g	1024 LSB/g
others	reserved	-

7.2 Self-Test

The self-test feature allows for checking the sensor functionality by applying electrostatic forces to the sensor core instead of external accelerations. By physically deflecting the seismic mass, the entire signal path of the sensor is tested. Activation of the self-test results in a static offset in the acceleration data. Any external acceleration or gravitational force which is applied to the sensor during a self-test will be observed in the sensor output as a superposition of the acceleration and the self-test signal.

Before enabling the self-test, the acceleration measurement range should be set to **4 g**.

The self-test is activated for **each axis separately** by setting bits <1:0> (*self_test_axis*) of register 0x32 (PMU_SELF_TEST) to 01 for the x-axis, 10 for the y-axis or 11 for the z-axis. For *self_test_axis* = 00, the self-test is disabled. The **direction of the deflection** is controlled via bit 2 (*self_test_sign*). The deflection is negative (positive) when setting *self_test_sign* to 0 (1).

After enabling the self-test, a **waiting time of 50 ms** is mandatory for each axis before the acceleration data are interpreted.

For a proper interpretation of the self-test signals, it is recommended to perform the self-test for both the positive and the negative direction and to then calculate the difference of the resulting acceleration values. The minimum difference for each axis is shown in the table below. The actually measured signal differences can be significantly larger.

	x-axis	y-axis	z-axis
minimum difference signal	800 mg	800 mg	400 mg

After performing a self-test, a reset of the device is recommended. If the reset cannot be performed, the following sequence must be kept to prevent unwanted interrupt generation:

A. Disable interrupts
B. Change parameters of interrupts
C. Wait for at least 50 ms
D. Enable desired interrupts

7.3 Fast Offset Compensation

The fast offset compensation is a one-shot process by which the compensation value is set in such a way that when added to the raw acceleration, the resulting acceleration value of each selected axis approaches the target value of 0 g. For fast offset compensation, the g-range of the SMA131 has to be set to 2 g.

During the compensation process, an average of 16 consecutive acceleration values is computed and the difference between the target value and the computed value is written to bits <7:0> (*offset_ x/y/z*) in registers 0x38 (OFC_OFFSET_X), 0x39 (OFC_OFFSET_Y), 0x3A (OFC_OFFSET_Z). These public registers are updated with the contents of the internal registers and can be read and over-written by the user.

The fast offset compensation is triggered for each axis individually by setting bits <6:5> (*cal_trigger*) in register 0x36 (OFC_CTRL) as shown in the following table.

cal_trigger	Selected Axis
00	none
01	x
10	y
11	z

Bits *cal_trigger* are write-only. Once triggered, the status of the fast offset compensation process is reflected in the status bit 4 (*cal_rdy*) in register 0x36 (OFC_CTRL). *cal_rdy* is 0 while the correction is in progress. Otherwise, it is 1. *cal_rdy* is 0 when *cal_trigger* is not 00.

The content of the fast offset compensation registers is reset to zero by writing 1 to bit 7 (*offset_reset*) in register 0x36 (OFC_CTRL).

The fast offset compensation should not be used during operation in low power mode 1. In the low power mode, the availability of necessary data for a proper function of the fast offset compensation is not fulfilled.

7.4 Interrupt Engine

7.4.1 Interrupt Controller

The SMA131 features four programmable interrupt engines. Each interrupt can be independently enabled and configured. If the trigger condition of an enabled interrupt is fulfilled, the corresponding status bit is set to 1 and the selected interrupt pin is activated. The SMA131 provides one interrupt pin, INT1. Interrupts can be freely mapped to this pin. The state of the interrupt pin is derived from a logic “or” combination of all interrupts mapped to it.

The interrupt status registers are updated when a new data word is written into the acceleration data registers. If an interrupt is disabled, all active status bits associated with it are immediately reset.

7.4.2 General Features

An interrupt is cleared depending on the selected interrupt mode, which is common to all interrupts. There are three different interrupt modes: non-latched, latched, and temporary. The behavior of the different interrupt modes is shown in Figure 27.

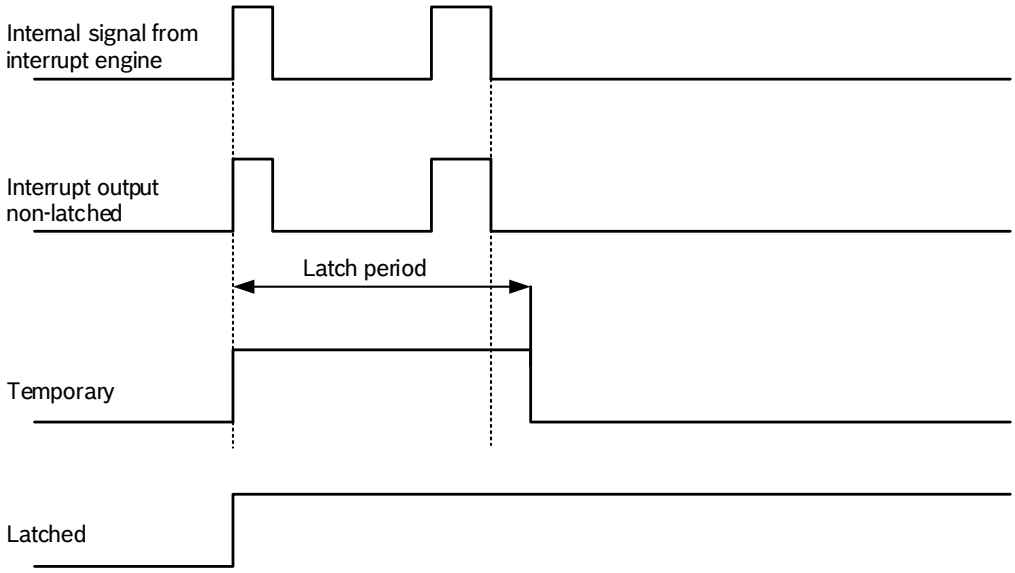


Figure 27 Interrupt modes

The mode is selected by the bits <3:0> (*latch_int*) in register 0x21 (INT_RST_LATCH) according to the following table.

latch_int	Interrupt Mode	latch_int	Interrupt Mode
0000	non-latched	1000	non-latched
0001	temporary, 250 ms	1001	temporary, 250 µs
0010	temporary, 500 ms	1010	temporary, 500 µs
0011	temporary, 1 s	1011	temporary, 1 ms
0100	temporary, 2 s	1100	temporary, 12.5 ms
0101	temporary, 4 s	1101	temporary, 25 ms
0110	temporary, 8 s	1110	temporary, 50 ms
0111	latched	1111	latched

An interrupt is generated if its activation condition is met. It cannot be cleared as long as the activation condition is fulfilled.

In the **non-latched** mode, the interrupt status bit and the selected pin (i.e., the contribution to the “or” condition for INT1) are cleared as soon as the activation condition is no more valid. Exceptions to this behavior is the new data interrupt, which is automatically reset after a fixed time.

In the **latched mode**, an asserted interrupt status and the selected pin are cleared by writing 1 to bit 7 (*reset_int*) in register 0x21 (INT_RST_LATCH). If the activation condition is still valid when the bit is cleared, the interrupt status is asserted again with the next change of the acceleration registers.

In the **temporary mode**, an asserted interrupt status and the selected pin are cleared after a defined period of time (selectable between 250 µs and 8 s).

Several interrupt engines can use either unfiltered or filtered acceleration data as their input. For these interrupts, the source can be selected with the bits <5:1> in register 0x1E (INT_SRC): *int_src_data*, *int_src_slo_no_mot*, *int_src_slope* and *int_src_high*. Setting the respective bits to 0 (1) selects filtered (unfiltered) data as input.

It is strongly recommended to set interrupt parameters prior to enabling the interrupt. Changing parameters of an already enabled interrupt may cause unwanted interrupt generation and generation of a false interrupt history. A safe way to change parameters of an enabled interrupt is to keep the following sequence:

- disable the desired interrupt
- change parameters
- wait for at least 10 ms
- re-enable the desired interrupt

7.4.3 Mapping to Interrupt Pin INT1

Registers 0x19 (INT_MAP_0) and 0x1A (INT_MAP_1) are dedicated to the mapping of interrupts to the interrupt pin INT1. Setting the respective bit (*int1_"inttype"*) in register 0x19 (INT_MAP_0) to 1 (0) maps (unmaps) *"inttype"* to pin INT1.

Note: *"inttype"* is to be replaced with the precise notation, given in the register map in section **Error! Reference source not found.**

7.4.4 Electrical Behavior of Interrupt Pin INT1

The interrupt pin INT1 can be configured to show the desired electrical behavior. The "active" level of the interrupt pin is determined by bit 0 (*int1_lvl*) in register 0x20 (INT_OUT_CTRL). If *int1_lvl* is 1 (0), then pin INT1 is active 1 (0).

The characteristics of the output driver of the interrupt pin may be configured with bit 1 (*int1_od*) in register 0x20 (INT_OUT_CTRL). By setting *int1_od* to 1, the output driver shows open-drive characteristics. By setting the bit to 0, the output driver shows push-pull characteristics. When open-drive characteristics are selected in the design, external pull-up or pull-down resistors should be applied according to the *int1_lvl* configuration.

7.4.5 New Data Interrupt

The new data interrupt serves for synchronous reading of acceleration data. It is generated after storing a new value of z-axis acceleration data in the data register. The interrupt is cleared automatically when the next data acquisition cycle starts. The interrupt status is 0 for at least 50 µs.

The interrupt mode of the new data interrupt is fixed to non-latched.

The new data interrupt is enabled (disabled) by writing 1 (0) to bit 4 (*data_en*) in register 0x17 (INT_EN_1). The interrupt status is stored in bit 7 (*data_int*) in register 0x0A (INT_STATUS_1).

Due to the filter settling time, the first interrupt after wake-up from suspend mode will take longer than the update time.

7.4.6 Slope / Any-Motion Detection

The slope / any-motion detection interrupt uses the slope between successive acceleration signals to detect changes in motion. An interrupt is generated when the slope (i.e., the absolute value of the acceleration difference) exceeds a configurable, preset threshold. It is cleared as soon as the slope falls below the threshold. The principle of the slope / any-motion interrupt is shown in Figure 28.

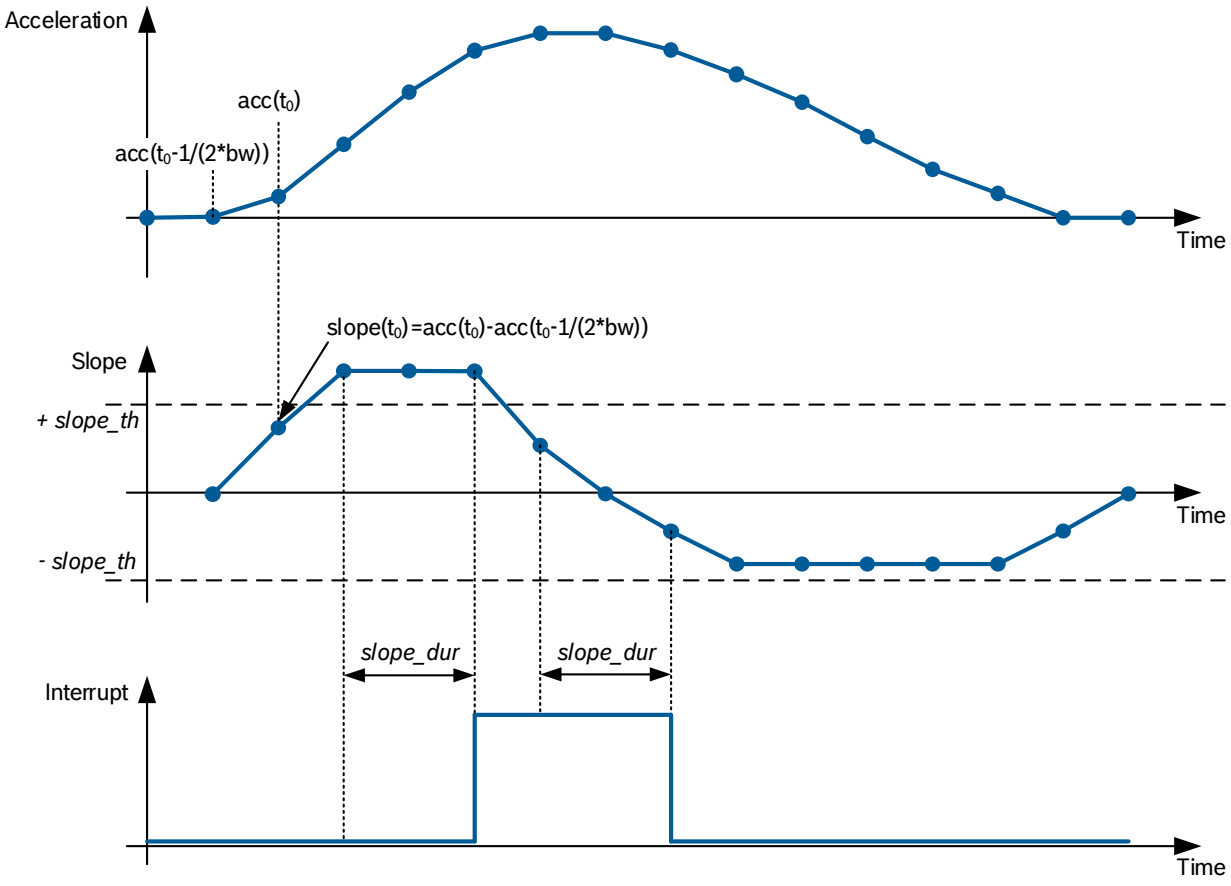


Figure 28 Principle of the slope / any-motion detection

The threshold is defined through register 0x28 (INT_6), bits <7:0> (*slope_th*). The scaling of 1 LSB of *slope_th* for the different g-ranges is given in the following table.

g-range	Scaling of 1 LSB of *slope_th*
2 g	3.91 mg
4 g	7.81 mg
8 g	15.6 mg

The time difference between the successive acceleration signals depends on the selected bandwidth and equates to

$$\Delta t = \frac{1}{2 \cdot bandwidth} .$$

In order to suppress false triggers, the interrupt is only generated (cleared) if a certain number *N* of consecutive slope data points is larger (smaller) than the slope threshold given by *slope_th*. This number is set by the bits <1:0> (*slope_dur*) in register 0x27 (INT_5) according to the following equation.

$$N = slope\_dur + 1$$

7.4.6.1 Enabling (Disabling) for Each Axis

Slope / any-motion detection can be enabled (disabled) for each axis separately by writing 1 (0) to bits 0 (*slope_en_x*), 1 (*slope_en_y*) or 2 (*slope_en_z*) in register 0x16 (INT_EN_0). The interrupt is generated if the slope of any of the enabled axes exceeds the threshold *slope_th* for *N* consecutive times. As soon as the slopes of all enabled axes fall or stay below this threshold for *N* consecutive times, the interrupt is cleared (unless the interrupt signal is latched).

7.4.6.2 Axis and Sign Information

The interrupt status is stored in bit 2 (*slope_int*) in register 0x09 (INT_STATUS_0). The slope / any-motion interrupt provides additional information about the detected slope. The axis which triggered the interrupt is given by bit 0 (*slope_first_x*), 1 (*slope_first_y*) or 2 (*slope_first_z*) in register 0x0B (INT_STATUS_2) which is set to 1. The sign of the triggering slope is kept in bit (*slope_sign*) in register 0x0B until the interrupt is retriggered. If *slope_sign* is 0 (1), the sign is positive (negative).

7.4.7 High-g Interrupt

The high-g interrupt is based on the comparison of acceleration data against a high-g threshold for the detection of wake-up, shock or other high-acceleration events.

The high-g interrupt is enabled (disabled) for each axis by writing 1 (0) to the respective bits 0 (*high_en_x*), 1 (*high_en_y*) or 2 (*high_en_z*) in register 0x17 (INT_EN_1). The high-g threshold is set via bits <7:0> (*high_th*) in register 0x26 (INT_4). The scaling of 1 LSB of *high_th* depends on the selected g-range and is summarized in the following table.

g-range	Scaling of 1 LSB of *high_th*
2 g	7.81 mg
4 g	15.63 mg
8 g	31.25 mg

A hysteresis can be selected by setting bits <7:6> (*high_hy*) in register 0x24 (INT_2). Analogously to *high_th*, the scaling of 1 LSB of *high_hy* depends on the selected g-range and is summarized in the following table.

g-range	Scaling of 1 LSB of *high_hy*
2 g	125 mg
4 g	250 mg
8 g	500 mg

The high-g interrupt is generated if the absolute value of the acceleration of at least one of the selected axes (“or” relation) is higher than the threshold for at least the time defined by the bits <7:0> (*high_dur*) in register 0x25 (INT_3). The relation between the content of *high_dur* and the actual delay of the interrupt generation is given by the following equation.

$$\text{delay [ms]} = \textit{high\_dur} \cdot 2 \text{ ms}$$

Note: *high_dur* = 0 is not specified and will lead to incorrect interrupt evaluation.

Thus, possible delay times range from 2 ms to 510 ms.

The interrupt is reset if the absolute value of the acceleration of all selected axes (“and” relation) is lower than the threshold minus the hysteresis for at least the time defined by *high_dur*. The interrupt status is stored in bit 1 (*high_int*) in register 0x09 (INT_STATUS_0). The high-g interrupt will be cleared immediately once the acceleration is lower than the threshold defined in *high_th*.

7.4.7.1 Axis and Sign Information

The axis which triggered the high-g interrupt is indicated by bits 0 (*high_first_x*), 1 (*high_first_y*) or 2 (*high_first_z*) in register 0x0C (INT_STATUS_3). The bit which corresponds to the triggering axis is set to 1 while the other bits are 0. These bits are cleared when the interrupt status is cleared. The sign of the triggering acceleration is stored in bit 3 (*high_sign*) in register 0x0C. If *high_sign* is 0 (1), the sign is positive (negative).

7.4.8 No-Motion / Slow-Motion Detection

The no-motion / slow-motion interrupt can be configured in two modes.

In **slow-motion** mode, an interrupt is triggered when the measured slope of at least one enabled axis exceeds the programmable slope threshold for a programmable number of samples. In order to suppress false triggers, the interrupt is only generated (cleared) if a certain number *N* of consecutive slope data points is larger (smaller) than the slope threshold defined by bits <3:2> (*slo_no_mot_dur* <1:0>) in register 0x27 (INT_5). *N* is given by the following equation.

$$N = slo\_no\_mot\_dur\ <1:0> + 1$$

In **no-motion mode**, an interrupt is generated if the slope of all selected axes remains smaller than a programmable threshold for a programmable delay time. The timing diagram for the no-motion interrupt is shown in Figure 29.

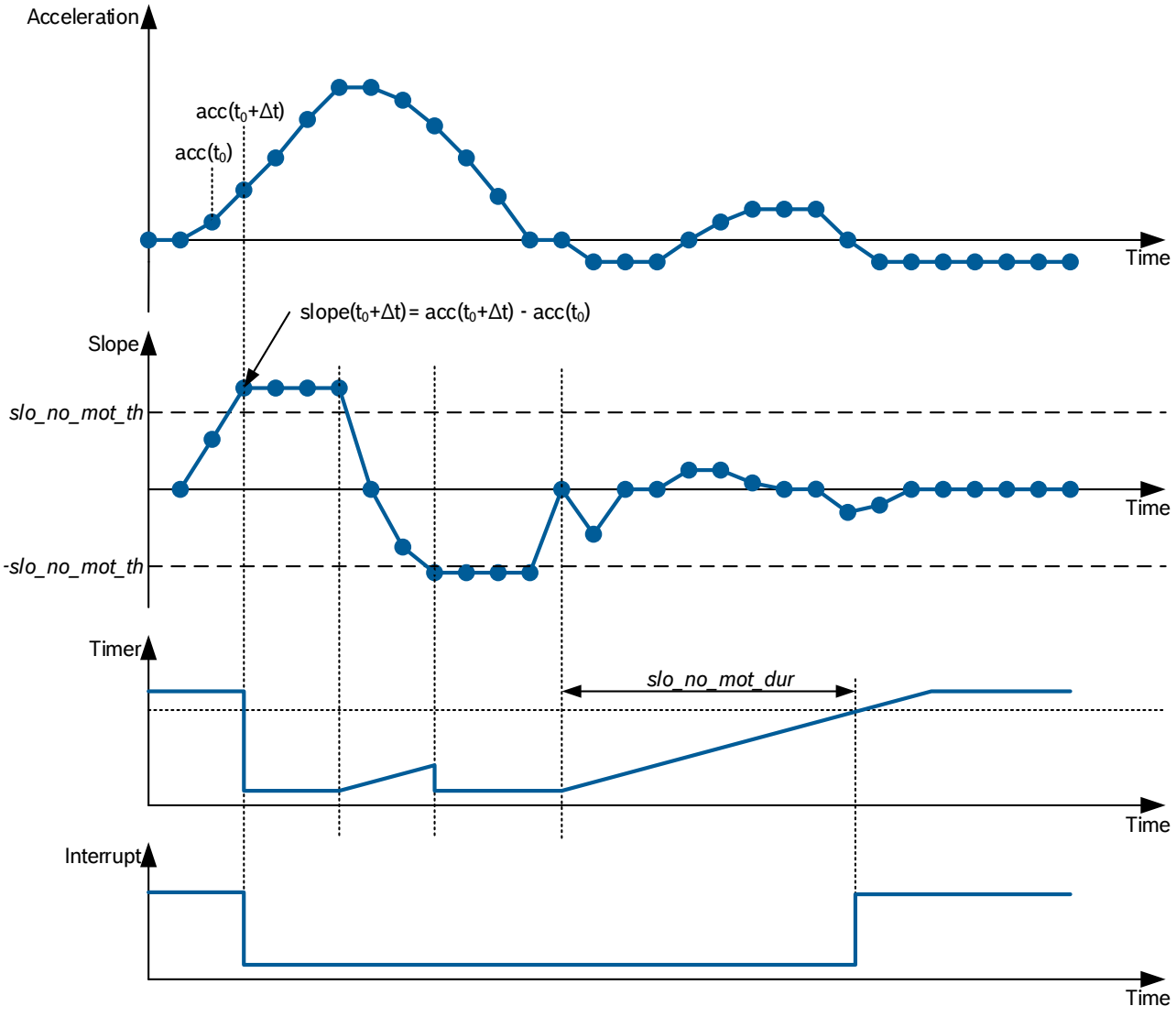


Figure 29 Timing of the no-motion interrupt

The scaling of the threshold value is identical to the one of the slow-motion interrupt. However, in no-motion mode, bits <7:2> (*slo_no_mot_dur* <5:0>) in register 0x27 define the delay time before the no-motion interrupt is triggered. The table below lists the delay times which can be set via *slo_no_mot_dur*. The timer tick period is 1 s. Thus, using short delay times can result in considerable timing uncertainties.

slo_no_mot_dur (DEC)	Delay Time	slo_no_mot_dur (DEC)	Delay Time	slow_no_mot_dur (DEC)	Delay Time
0	1 s	16	40 s	32	88 s
1	2 s	17	48 s	33	96 s
2	3 s	18	56 s	34	104 s
...	...	19	64 s	...	...
14	15 s	20	72 s	62	328 s
15	16 s	21	80 s	63	336 s

Note: *slo_no_mot_dur* values 22 to 31 are not specified.

The delay times can be calculated with the help of the following equations:

slo_no_mot_dur <5:4> = 00: delay time = *slo_no_mot_dur* <3:0> + 1

slo_no_mot_dur <5:4> = 01: delay time = *slo_no_mot_dur* <3:0> · 8 + 40

slo_no_mot_dur <5> = 1: delay time = *slo_no_mot_dur* <4:0> · 8 + 88

The no-motion / slow-motion mode selection takes place via bit 3 (*slo_no_mot_sel*) in register 0x18 (INT_EN_2). If *slo_no_mot_sel* is set to 1 (0), the no-motion (slow-motion) mode is selected. In both modes, the slopes of the axes are monitored which have been enabled via bits 0 (*slo_no_mot_en_x*), 1 (*slo_no_mot_en_y*) and 2 (*slo_no_mot_en_z*) in register 0x18. The measured slope values are continuously compared against the threshold value defined by bits <7:0> (*slo_no_mot_th*) in register 0x29 (INT_7). The scaling of 1 LSB of *slo_no_mot_th* for the different g-ranges and the corresponding maximum value is given by the table below.

g-range	Scaling of 1 LSB of *slo_no_mot_th*	Maximum Value
2 g	3.91 mg	996 mg
4 g	7.81 mg	1.99 g
8 g	15.6 mg	3.98 g

The time difference between the successive acceleration samples depends on the selected filter bandwidth and is given by 1/(2·bandwidth). The interrupt status is stored in bit 3 (*slo_no_mot_int*) in register 0x09 (INT_STATUS_0).

NOTE: The no-motion interrupt can only be used in non-latched or latched mode and not in temporary latch.

NOTE: When using the no-motion interrupt in combination with a low power mode, please consider your bosch representative.

7.5 Power Modes

The SMA131 offers four different power modes. Besides the normal mode, which represents the fully operational state of the SMA131, there are three power saving modes for power-critical applications: suspend mode, deep suspend mode and low power mode 1.

The possible transitions between the different power modes are shown in Figure 30.

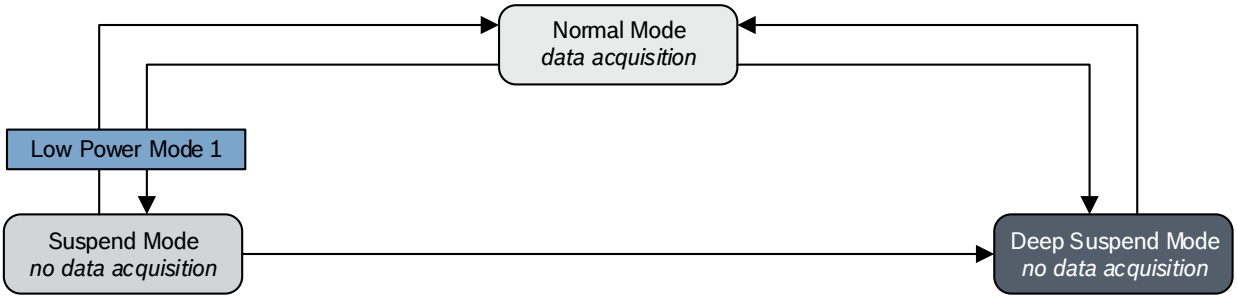


Figure 30 SMA131 power modes

After power-up, the SMA131 is in **normal mode**. Here, all parts of the device are held powered up and data acquisition is performed continuously.

In **suspend mode**, the whole analog part of the SMA131 is powered down. Here, no data acquisition is performed. While in suspend mode, the latest acceleration data and the content of all configuration registers are kept. Writing to and reading from registers is supported. However, an idle time of at least 450 µs is required between two consecutive write cycles (see section 6.3)

The suspend mode is entered (left) by writing 0 to bit 6 (*lowpower_mode*) in register 0x12 (PMU_LOW_POWER) and writing 1 (0) to bit 7 (*suspend*) in register 0x11 (PMU_LPW). From the suspend mode, it is also possible to enter the normal mode by performing a soft reset (see section 7.7).

In **deep suspend mode**, the SMA131 reaches the lowest possible power consumption. Only the interface section is kept alive. Here, no data acquisition is performed. The content of all configuration registers is lost. All application specific settings which are not equal to the default settings must be reset to their designated values after leaving the deep suspend mode.

The TWI watchdog timer remains functional. The bit (*deep_suspend*) in register 0x11 (PMU_LPW) and the bits 2 (*i2c_wdt_en*) and 1 (*i2c_wdt_sel*) in register 0x34 (BGW_SPI3_WDT) also remain functional in deep suspend mode. The interrupt level and driver configuration bits 0 (*int1_lvl*) and 1 (*int1_od*) in register 0x20 (INT_OUT_CTRL) are still accessible.

The deep suspend mode is entered (left) by writing 1 (0) to bit 5 (*deep_suspend*) in register 0x11 (PMU_LPW) while bit 7 (*suspend*) is set to 0. From the deep suspend mode, it is also possible to enter the normal mode by performing a soft reset (see s

ection 7.7).

In **low power mode 1**, the SMA131 is periodically switching between a power saving sleep phase and a wake-up phase, in which data acquisition takes place. The wake-up phase corresponds to operation in normal mode with the complete circuitry powered up. The sleep phase corresponds to operation in suspend mode. Read access to registers is possible. However, unless the register access is synchronized with the wake-up phase, the restrictions of the suspend mode apply.

The low power mode 1 is entered (left) by writing 0 to bit 6 (*lowpower_mode*) in register 0x12 (PMU_LOW_POWER) and writing 1 (0) to bit 6 (*lowpower_en*) in register 0x11 (PMU_LPW).

An **overview** of the register configurations of 0x11 (PMU_LPW) and 0x12 (PMU_LOW_POWER) for entering normal mode, suspend mode, deep suspend mode and low power mode 1 is given in the following table.

Mode	0x11 (PMU_LPW)			0x12 (PMU_LOW_POWER)
	7 *suspend*	*6* *lowpower_en*	*5* *deep_suspend*	*6* *lowpower_mode*
Normal	0	0	0	0
Suspend	1	0	0	0
Deep suspend	0	0	1	0
Low power mode 1	0	1	0	0

The **timing behavior** of low power mode 1 is event-driven. The duration of the wake-up phase depends on the number of samples which are required by the enabled interrupt engines. If an interrupt is detected, the SMA131 stays in the wake-up phase as long as the interrupt conditions endure (non-latched interrupt), until the latch time expires (temporary interrupt) or until the interrupt is reset (latched interrupt). If no interrupt is detected, the SMA131 enters the sleep phase immediately after the required number of acceleration samples have been taken and an active interface access cycle has ended. The timing diagram of low power mode 1 is shown in Figure 31.

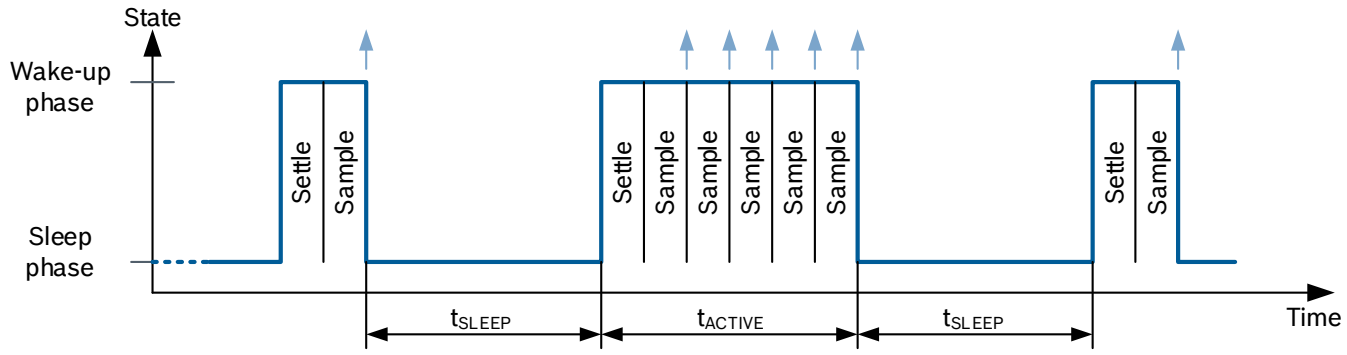


Figure 31 Timing diagram for low power mode 1

The **sleep time** for low power mode 1 is set by bits <4:1> (*sleep_dur*) in register 0x11 (PMU_LPW) according to the following table.

sleep_dur	Sleep Phase Duration (t_{sleep})	sleep_dur	Sleep Phase Duration (t_{sleep})
0000	0.5 ms	1000	4 ms
0001	0.5 ms	1001	6 ms
0010	0.5 ms	1010	10 ms
0011	0.5 ms	1011	25 ms
0100	0.5 ms	1100	50 ms
0101	0.5 ms	1101	100 ms
0110	1 ms	1110	500 ms
0111	2 ms	1111	1 s

The **current consumption** of the SMA131 in low power mode 1 (I_{DDlp1}) can be estimated with the following equation:

$$I_{DDlp1} \approx \frac{t_{sleep} \cdot I_{DDsum} + t_{active} \cdot I_{DD}}{t_{sleep} + t_{active}}$$

For the estimation of the duration of the wake-up phase t_{active}, the corresponding wake-up time $t_{w,up1}$ and the filter update time t_{ut} have to be considered.

If the bandwidth is ≥ 31.25 Hz, t_{active} is given by:

$$t_{active} = t_{ut} + t_{w,up1/2} - 0.9ms$$

Else, t_{active} is given by:

$$t_{active} = 4 \cdot t_{ut} + t_{w,up1/2} - 0.9ms$$

The filter update times t_{ut} are given by the following table.

bw	Bandwidth	Update Time (t_{ut})
00xxx	*)	-
01000	7.81 Hz	64 ms
01001	15.63 Hz	32 ms
01010	31.25 Hz	16 ms
01011	62.5 Hz	8 ms
01100	125 Hz	4 ms
01101	250 Hz	2 ms
01110	500 Hz	1 ms
01111	1000 Hz	0.5 ms
1xxxx	*)	-

*) The *bw* settings 00xxx and 1xxxx are both reserved. *bw* = 00xxx results in a bandwidth of 7.81 Hz, *bw* = 1xxxx results in an unfiltered signal. It is recommended to actively set an appropriate, application specific bandwidth and to use the *bw* range from 01000 to 01111.

During the wake-up phase, all analog modules are held powered up, while during the sleep phase, most analog modules are powered down. Consequently, a wake-up time of at least $t_{w,up1}$ is needed to settle the analog modules so that reliable acceleration data are generated.

7.6 Reading Data

The data representation of the SMA131 follows two's complement representation.

For each axis, the 14 bits of acceleration data are split into a MSB upper part (one byte containing bits <13:6> of acceleration data) and a LSB lower part (one byte containing bits <5:0> of acceleration data, one *undefined* bit with random data which is to be ignored and a *new_data* flag). Registers 0x02 (ACCD_X_LSB) and 0x03 (ACCD_X_MSB) contain the acceleration data for the x-channel, registers 0x04 (ACCD_Y_LSB) and 0x05 (ACCD_Y_MSB) for the y-channel and 0x06 (ACCD_Z_LSB) and 0x07 (ACCD_Z_MSB) for the z-channel. It is recommended to always start reading out the acceleration data registers with the LSB part first.

An example for the range setting of ±2 g is shown in the table below.

LSB	1111 11xx		0000 00xx		0000 00xx
MSB	0111 1111		0000 0000		1000 0000
MSB + LSB [bin]	0111 1111 111111		0000 0000 000000		1000 0000 000000
MSB + LSB [dec]	+8191	...	0	...	-8192
Acceleration value	+2 g	...	0 g	...	-2 g

In order to ensure data integrity, a **shadowing procedure** can be enabled. In this case, the content of the MSB register is locked by reading the corresponding LSB register until the MSB register is read as well. This means that the MSB register always has to be read in order to remove the data lock. Shadowing can be disabled (enabled) by writing 1 (0) to bit 6 (*shadow_dis*) in the register 0x13 (ACCD_HBW). For disabled shadowing, the content of both the MSB and the LSB register is updated by new values immediately. Unused bits of the LSB registers may have any value and should be ignored.

New data can be identified by bit 0 (*new_data* flag) of each LSB register. It is set if the data registers have been updated and reset if either the corresponding MSB or LSB part is read.

Two different streams of acceleration data are available, **unfiltered and filtered** data. The unfiltered data is sampled with 2 kHz. The sampling rate (output data rate ODR) of the filtered data depends on the selected filter bandwidth (BW) and is always twice the selected bandwidth (BW = ODR/2). Which kind of data is stored in the acceleration data registers depends on bit 7 (*data_high_bw*) in register 0x13 (ACCD_HBW). If bit 7 is 0 (1), filtered (unfiltered) data is stored in the registers. Both data streams are offset-compensated.

7.7 Soft Reset

A soft reset causes all user configuration settings to be overwritten with their default values and the sensor to enter normal mode.

A soft reset is initiated by writing the value 0xB6 to register 0x14 (BGW_SOFTRESET).

7.8 Register Map

The entire communication with the device is performed by reading from and writing to registers. Registers have a width of 8 bits. They are mapped to a common space of 64 addresses from 0x00 up to 0x3F. Within this range some registers are either completely or partially marked as ‘reserved’. Any reserved bit is ignored when it is written and no specific value is guaranteed when the bit is read. It is recommended not to use registers which are completely marked as ‘reserved’ at all. Furthermore it is recommended to mask out (logical and with zero) reserved bits of registers which are partially marked as reserved.

Registers with addresses from 0x00 up to 0x0E are read-only. Any attempt to write to those registers will be ignored. There are bits within some registers that trigger internal sequences. These bits are configured for write-only access and read as 0. An example for such a write-only access is the entire register 0x14 (BGW_SOFTRESET).

Figure 32 shows the register map of the SMA131.

Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Default
0x3A	offset_z<7:0>								0x00
0x39	offset_y<7:0>								0x00
0x38	offset_x<7:0>								0x00
0x36	offset_reset	cal_trigger<1:0>		cal_rdy					0x10
0x34						i2c_wdt_en	i2c_wdt_sel		0x00
0x32						self_test_sign	self_test_axis<1:0>		0x00
0x29	slo_no_mot_th<7:0>								0x14
0x28	slope_th<7:0>								0x14
0x27	slo_no_mot_dur<5:0>						slope_dur<1:0>		0x00
0x26	high_th<7:0>								0xC0
0x25	high_dur<7:0>								0x0F
0x24	high_hy<1:0>								0x81
0x21	reset_int				latch_int<3:0>				0x00
0x20							int1_od	int1_lvl	0x05
0x1E			int_src_data		int_src_slo_no_mot	int_src_slope	int_src_high		0x00
0x1A								int1_data	0x00
0x19					int1_slo_no_mot	int1_slope	int1_high		0x00
0x18					slo_no_mot_sel	slo_no_mot_en_z	slo_no_mot_en_y	slo_no_mot_en_x	0x00
0x17				data_en		high_en_z	high_en_y	high_en_x	0x00
0x16						slope_en_z	slope_en_y	slope_en_x	0x00
0x14	softreset								0x00
0x13	data_high_bw	shadow_dis							0x00
0x12		lowpower_mode							0x00
0x11	suspend	lowpower_en	deep_suspend	sleep_dur<3:0>					0x00
0x10				bw <4:0>					0x0F
0x0F					range <3:0>				0x03
0x0C					high_sign	high_first_z	high_first_y	high_first_x	0x00
0x0B					slope_sign	slope_first_z	slope_first_y	slope_first_x	0x00
0x0A	data_int								0x00
0x09					slo_no_mot_int	slope_int	high_int		0x00
0x07	acc_z_msb <13:6>								0x00
0x06	acc_z_lsb <5:0>							new_data_z	0x00
0x05	acc_y_msb <13:6>								0x00
0x04	acc_y_lsb <5:0>							new_data_y	0x00
0x03	acc_x_msb <13:6>								0x00
0x02	acc_x_lsb <5:0>							new_data_x	0x00
0x00	chip_id <7:0>								0xFB

	write / read access
	write access only
	ready access only
0xXY	*Common w/r registers: Application specific settings not equal to default. Must be reset to designated values after POR, soft reset and wake-up from deep suspend.*
0xXY	*User w/r registers: Initial default content = 0x00. Freely programmable by user.*
	reserved

Figure 32 SMA131 register map

7.8.1 Register 0x00 (BGW_CHIPID)

This register contains the chip identification code.

0x00	BGW_CHIPID							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*chip_id* <7:0>							

Register	Description
chip_id <7:0>	Fixed value 11111000

7.8.2 Register 0x02 (ACCD_X_LSB)

This register contains the least significant bits of the x-channel acceleration readout value. When reading out x-channel acceleration values, data consistency is guaranteed if the ACCD_X_LSB is read out before the ACCD_X_MSB and *shadow_dis* = 0. In this case, after the ACCD_X_LSB has been read, the value in the ACCD_X_MSB register is locked until the ACCD_X_MSB has been read. Acceleration data may be read from register ACCD_X_LSB at any time except during power-up and in deep suspend mode.

0x02	ACCD_X_LSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*acc_x_lsb* <5:0>						*undefined*	*new_data_x*

Register	Description
acc_x_lsb <5:0>	Least significant 6 bits of the acceleration x-channel read-back value (two's complement format)
undefined	Random data, to be ignored
new_data_x	0: acceleration value has not been updated since it has been read out last 1: acceleration value has been updated since it has been read out last

7.8.3 Register 0x03 (ACCD_X_MSB)

This register contains the most significant bits of the x-channel acceleration readout value. When reading out x-channel acceleration values, data consistency is guaranteed if the ACCD_X_LSB is read out before the ACCD_X_MSB and *shadow_dis* = 0. In this case, after the ACCD_X_LSB has been read, the value in the ACCD_X_MSB register is locked until the ACCD_X_MSB has been read. Acceleration data may be read from register ACCD_X_MSB at any time except during power-up and in deep suspend mode.

0x03	ACCD_X_MSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*acc_x_msb* <13:6>							

Register	Description
acc_x_msb <13:6>	Most significant 8 bits of the acceleration x-channel read-back value (two's complement format)

7.8.4 Register 0x04 (ACCD_Y_LSB)

This register contains the least significant bits of the y-channel acceleration readout value. When reading out y-channel acceleration values, data consistency is guaranteed if the ACCD_Y_LSB is read out before the ACCD_Y_MSB and *shadow_dis* = 0. In this case, after the ACCD_Y_LSB has been read, the value in the ACCD_Y_MSB register is locked until the ACCD_Y_MSB has been read. Acceleration data may be read from register ACCD_Y_LSB at any time except during power-up and in deep suspend mode.

0x04	ACCD_Y_LSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*acc_y_lsb* <5:0>						*undefined*	*new_data_y*

Register	Description
acc_y_lsb <5:0>	Least significant 6 bits of the acceleration y-channel read-back value (two's complement format)
undefined	Random data, to be ignored
new_data_y	0: acceleration value has not been updated since it has been read out last 1: acceleration value has been updated since it has been read out last

7.8.5 Register 0x05 (ACCD_Y_MSB)

This register contains the most significant bits of the y-channel acceleration readout value. When reading out y-channel acceleration values, data consistency is guaranteed if the ACCD_Y_LSB is read out before the ACCD_Y_MSB and *shadow_dis* = 0. In this case, after the ACCD_Y_LSB has been read, the value in the ACCD_Y_MSB register is locked until the ACCD_Y_MSB has been read. Acceleration data may be read from register ACCD_Y_MSB at any time except during power-up and in deep suspend mode.

0x05	ACCD_Y_MSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*acc_y_msb* <13:6>							

Register	Description
acc_y_msb <13:6>	Most significant 8 bits of the acceleration y-channel read-back value (two's complement format)

7.8.6 Register 0x06 (ACCD_Z_LSB)

This register contains the least significant bits of the z-channel acceleration readout value. When reading out z-channel acceleration values, data consistency is guaranteed if the ACCD_Z_LSB is read out before the ACCD_Z_MSB and *shadow_dis* = 0. In this case, after the ACCD_Z_LSB has been read, the value in the ACCD_Z_MSB register is locked until the ACCD_Z_MSB has been read. Acceleration data may be read from register ACCD_Z_LSB at any time except during power-up and in deep suspend mode.

0x06	ACCD_Z_LSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*acc_z_lsb* <5:0>						*undefined*	*new_data_z*

Register	Description
acc_z_lsb <5:0>	Least significant 6 bits of the acceleration z-channel read-back value (two's complement format)
undefined	Random data, to be ignored

new_data_y	0: acceleration value has not been updated since it has been read out last 1: acceleration value has been updated since it has been read out last

7.8.7 Register 0x07 (ACCD_Z_MSB)

This register contains the most significant bits of the z-channel acceleration readout value. When reading out z-channel acceleration values, data consistency is guaranteed if the ACCD_Z_LSB is read out before the ACCD_Z_MSB and *shadow_dis* = 0. In this case, after the ACCD_Z_LSB has been read, the value in the ACCD_Z_MSB register is locked until the ACCD_Z_MSB has been read. Acceleration data may be read from register ACCD_Z_MSB at any time except during power-up and in deep suspend mode.

0x07	*ACCD_Z_MSB*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*acc_z_msb* <13:6>							

Register	Description
acc_z_msb <13:6>	Most significant 8 bits of the acceleration z-channel read-back value (two's complement format)

7.8.8 Register 0x09 (INT_STATUS_0)

This register contains the interrupt status flags *slo_no_mot_int*, *slope_int* and *high_int*. Each flag is associated with a specific interrupt function. It is set when the associated interrupt triggers.

The setting of the bits <3:0> (*latch_int*) in register 0x21 (INT_RST_LATCH) controls if the interrupt signal and hence the respective interrupt flag will be permanently latched, temporarily latched or non-latched.

The interrupt function associated with a specific status flag has to be enabled separately.

0x09	INT_STATUS_0							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*reserved*				*slo_no_mot_int*	*slope_int*	*high_int*	*reserved*

Register	Description
slo_no_mot_int	Slow / no-motion interrupt status 0: inactive 1: active
slope_int	Slope interrupt status 0: inactive 1: active
high_int	High-g interrupt status 0: inactive 1: active
reserved	Random data, to be ignored

7.8.9 Register 0x0A (INT_STATUS_1)

This register contains the interrupt status flag *data_int* of the new data interrupt.

The new data interrupt allows for synchronous reading of acceleration data. It is generated after a new value of z-axis acceleration data has been stored in the data register.

The interrupt is cleared automatically when the next data acquisition cycle starts. The interrupt status is 0 for a minimum of 50 µs. It is fixed to the non-latched mode.

The interrupt function associated with the status flag has to be enabled via setting bit 4 (*data_en*) in register 0x17 (INT_EN_1) to 1.

0x0A	*INT_STATUS_1*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*data_int*	*reserved*						

Register	Description
data_int	Data ready interrupt status 0: inactive 1: active
reserved	Random data, to be ignored

7.8.10 Register 0x0B (INT_STATUS_2)

This register contains the interrupt status flags *slope_sign*, *slope_first_z*, *slope_first_y* and *slope_first_x*. Each flag is associated with a specific interrupt function. It is set when the associated interrupt triggers.

The setting of the bits <3:0> (*latch_int*) in register 0x21 (INT_RST_LATCH) controls if the interrupt signal and hence the respective interrupt flag will be permanently latched, temporarily latched or non-latched.

The interrupt function associated with a specific status flag has to be enabled separately.

0x0B	INT_STATUS_2							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*reserved*				*slope_sign*	*slope_first_z*	*slope_first_y*	*slope_first_x*

Register	Description
slope_sign	Slope sign of the slope triggering signal was 0: positive 1: negative
slope_first_z	Slope interrupt was 0: not triggered by z-axis 1: triggered by z-axis
slope_first_y	Slope interrupt was 0: not triggered by y-axis 1: triggered by y-axis
slope_first_x	Slope interrupt was 0: not triggered by x-axis 1: triggered by x-axis
reserved	Random data, to be ignored

7.8.11 Register 0x0C (INT_STATUS_3)

This register contains the interrupt status flags *high_sign*, *high_first_z*, *high_first_y* and *high_first_x.* Each flag is associated with a specific interrupt function. It is set when the associated interrupt triggers.

The setting of the bits <3:0> (*latch_int*) in register 0x21 (INT_RST_LATCH) controls if the interrupt signal and hence the respective interrupt flag will be permanently latched, temporarily latched or non-latched.

The interrupt function associated with a specific status flag has to be enabled separately.

0x0C	INT_STATUS_3							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*reserved*				*high_sign*	*high_first_z*	*high_first_y*	*high_first_x*

Register	Description
high_sign	Sign of the acceleration signal that triggered the high-g interrupt was 0: positive 1: negative
high_first_z	High-g interrupt was 0: not triggered by z-axis 1: triggered by z-axis
high_first_y	High-g interrupt was 0: not triggered by y-axis 1: triggered by y-axis
high_first_x	High-g interrupt was 0: not triggered by x-axis 1: triggered by x-axis
reserved	Random data, to be ignored

7.8.12 Register 0x0F (PMU_RANGE)

This register allows for the selection of the accelerometer g-range.

0x0F	*PMU_RANGE*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	1
Content	*reserved*				*range* <3:0>			

Register	Description
range <3:0>	Selection of the accelerometer g-range *range* <3:0> | g-range | Resolution [LSB/g] 0011 | ±2 g | 4096 0101 | ±4 g | 2048 1000 | ±8 g | 1024 All other settings: reserved (do not use)
reserved	Write 0

7.8.13 Register 0x10 (PMU_BW)

This register allows for the selection of the acceleration data filter bandwidth.

0x10	PMU_BW							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	1	1	1
Content	*reserved*			*bw* <4:0>				

Register	Description
bw <4:0>	Selection of the data filter bandwidth:

bw <4:0>	Bandwidth	*bw* <4:0>	Bandwidth
00xxx	7.81 Hz	01100	125 Hz
01000	7.81 Hz	01101	250 Hz
01001	15.63 Hz	01110	500 Hz
01010	31.25 Hz	01111	ODR_{max}
01011	62.50 Hz	1xxxx	ODR_{max}

reserved	Write 0

7.8.14 Register 0x11 (PMU_LPW)

This register allows for the selection of the main power modes – in combination with register 0x12 (PMU_LOW_POWER) – and the low power mode sleep period.

Name	0x11 (PMU_LPW)							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*suspend*	*lowpower_en*	*deep_suspend*	*sleep_dur* <3:0>				reserved

Register	Description
suspend, *lowpower_en*, *deep_suspend*	Main power mode configuration setting 000: normal mode 001: deep suspend mode 010: low power mode 1 100: suspend mode All other settings: illegal (do not use) Please note that only certain power mode transitions are permitted.
sleep_dur <3:0>	Sleep phase duration in low power mode 1 0000 to 0101: 0.5 ms 0110: 1 ms 0111: 2 ms 1000: 4 ms 1001: 6 ms 1010: 10 ms 1011: 25 ms 1100: 50 ms 1101: 100 ms 1110: 500 ms 1111: 1 s
reserved	Write 0

Please note that all application specific settings which are not equal to the default settings must be reset to their designated values after leaving deep suspend mode.

7.8.15 Register 0x12 (PMU_LOW_POWER)

This register – in combination with register 0x11 (PMU_LPW) – contains the configuration settings for the main power modes.

0x12	PMU_LOW_POWER							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*	*lowpower_mode*	*reserved*					

Register	Description
lowpower_mode	Power mode configuration 0: low power mode 1, normal mode, suspend mode, deep suspend mode 1: illegal (do not use)
reserved	Write 0

Overview of the different configurations of register 0x11 (PMU_LPW) and 0x12 (PMU_LOW_POWER):

Mode	0x11 (PMU_LPW)			0x12 (PMU_LOW_POWER)
	7 *suspend*	6 *lowpower_en*	5 *deep_suspend*	6 *lowpower_mode*
Normal	0	0	0	0
Suspend	1	0	0	0
Deep suspend	0	0	1	0
Low power mode 1	0	1	0	0

7.8.16 Register 0x13 (ACCD_HBW)

This register controls the acceleration data acquisition and data output format.

0x13	*ACCD_HBW*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*data_high_bw*	*shadow_dis*	*reserved*					

Register	Description
data_high_bw	Data-read from the acceleration data registers 1: unfiltered 0: filtered
shadow_dis	The shadowing mechanism for the acceleration data output registers. When shadowing is enabled, the content of the acceleration data component in the MSB register is locked when the component in the LSB is read, thereby ensuring the integrity of the acceleration data during read-out. The lock is removed when the MSB is read. 1: disable 0: enable
reserved	Write 0

7.8.17 Register 0x14 (BGW_SOFTRESET)

This register controls the user triggered soft reset of the sensor.

0x14	BGW_SOFTRESET							
Bit	7	6	5	4	3	2	1	0
Read/Write	W	W	W	W	W	W	W	W
Reset Value	0	0	0	0	0	0	0	0
Content	*softreset*							

Register	Description
softreset	Writing 0xB6 to the register triggers a reset. Other values are ignored. After a delay, all user configuration settings are overwritten with their default values. This register is functional in all operation modes. Please note that all application spe-cific settings which are not equal to the default settings (refer to the register map in section(7.8) must be reconfigured to their designated values.

7.8.18 Register 0x16 (INT_EN_0)

This register controls if the slope / any-motion detection is enabled.

0x16	INT_EN_0							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*					*slope_en_z*	*slope_en_y*	*slope_en_x*

Register	Description
slope_en_z	z-axis component of the slope / any-motion interrupt is 0: disabled 1: enabled
slope_en_y	y-axis component of the slope / any-motion interrupt is 0: disabled 1: enabled
slope_en_x	x-axis component of the slope / any-motion interrupt is 0: disabled 1: enabled
reserved	Write 0

7.8.19 Register 0x17 (INT_EN_1)

This register controls which of the interrupts new data or high-g are enabled.

0x17	INT_EN_1							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*			*data_en*	*reserved*	*high_en_z*	*high_en_y*	*high_en_x*

Register	Description
data_en	New data interrupt is 0: disabled 1: enabled
high_en_z	z-axis component of the high-g interrupt is 0: disabled 1: enabled
high_en_y	y-axis component of the high-g interrupt is 0: disabled 1: enabled
high_en_x	x-axis component of the high-g interrupt is 0: disabled 1: enabled
reserved	Write 0

7.8.20 Register 0x18 (INT_EN_2)

This register controls the settings of the no-motion / slow-motion interrupt.

0x18	INT_EN_2							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*				*slo_no_mot_sel*	*slo_no_mot_en_z*	*slo_no_mot_en_y*	*slo_no_mot_en_x*

Register	Description
slo_no_mot_sel	Select 0: slow-motion interrupt function 1: no-motion interrupt function
slo_no_mot_en_z	z-axis component of the no-motion / slow-motion interrupt is 0: disabled 1: enabled
slo_no_mot_en_y	y-axis component of the no-motion / slow-motion interrupt is 0: disabled 1: enabled
slo_no_mot_en_x	x-axis component of the no-motion / slow-motion interrupt is 0: disabled 1: enabled
reserved	Write 0

7.8.21 Register 0x19 (INT_MAP_0)

This register controls which of the interrupts no-motion / slow-motion, slope / any-motion and high-g are mapped to the INT1 pin.

0x19	INT_MAP_0							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*				*int1_slo_no_mot*	*int1_slope*	*int1_high*	*reserved*

Register	Description
int1_slo_no_mot	Mapping of no-motion / slow motion interrupt to INT1 pin is 0: disabled 1: enabled
int1_slope	Mapping of slope / any-motion interrupt to INT1 pin is 0: disabled 1: enabled
int1_high	Mapping of high-g interrupt to INT1 pin is 0: disabled 1: enabled
reserved	Write 0

7.8.22 Register 0x1A (INT_MAP_1)

This register controls if the new data interrupt is mapped to the INT1 pin.

0x1A	INT_MAP_1							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*							*int1_data*

Register	Description
int1_data	Mapping of new data interrupt to INT1 pin is 0: disabled 1: enabled
reserved	Write 0

7.8.23 Register 0x1E (INT_SRC)

This register controls the data source definition for interrupts with selectable data source.

0x1E	INT_SRC							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*		*int_src_data*	*reserved*	*int_src_slo_no_mot*	*int_src_slope*	*int_src_high*	*reserved*

Register	Description
int_src_data	Data for new data interrupt are 0: filtered 1: unfiltered
int_src_slo_no_mot	Data for no-motion / slow-motion interrupt are 0: filtered 1: unfiltered
int_src_slope	Data for slope / any-motion interrupt are 0: filtered 1: unfiltered
int_src_high	Data for high-g interrupt are 0: filtered 1: unfiltered
reserved	Write 0

7.8.24 Register 0x20 (INT_OUT_CTRL)

This register controls the electrical behavior and configuration of the interrupt pins.

0x20	INT_OUT_CTRL							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	1
Content	*reserved*						*int1_od*	*int1_lvl*

Register	Description
int1_od	Behavior for the INT1 pin is 0: push-pull 1: open drain
int1_lvl	Level for the INT1 pin is 0: active low 1: active high
reserved	Write 0

7.8.25 Register 0x21 (INT_RST_LATCH)

This register contains the interrupt reset bit and the interrupt mode selection.

0x21	INT_RST_LATCH							
Bit	7	6	5	4	3	2	1	0
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reset_int*	*reserved*			*latch_int* <3:0>			

Register	Description
reset_int	Latched interrupts are 0: kept active 1: cleared
latch_int <3:0>	Interrupt mode 0000: non-latched 0001: temporary, 250 ms 0010: temporary, 500 ms 0011: temporary, 1 s 0100: temporary, 2 s 0101: temporary, 4 s 0110: temporary, 8 s 0111: latched 1000: non-latched 1001: temporary, 250 µs 1010: temporary, 500 µs 1011: temporary, 1 ms 1100: temporary, 12.5 ms 1101: temporary, 25 ms 1110: temporary, 50 ms 1111: latched
reserved	Write 0

7.8.26 Register 0x24 (INT_2)

This register contains the high_g interrupt hysteresis setting.

0x24	INT_2							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	1
Content	*high_hy* <1:0>		*reserved*					

Register	Description
high_hy <1:0>	Hysteresis of the high-g interrupt Scaling of 1 LSB of *high_hy*: 2 g-range: hysteresis = *high_hy* <1:0> · 125 mg 4 g-range: hysteresis = *high_hy* <1:0> · 250 mg 8 g-range: hysteresis = *high_hy* <1:0> · 500 mg
reserved	Write 0

7.8.27 Register 0x25 (INT_3)

This register contains the delay time definition of the high-g interrupt.

0x25	INT_3							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	1	1	1
Content	*high_dur* <7:0>							

Register	Description
high_dur <7:0>	High-g interrupt trigger delay delay = *high_dur* <7:0> · 2 ms **Note:** *high_dur* = 0 is not specified and will lead to incorrect interrupt evaluation. The range is from 2 ms to 510 ms, with a default setting of 30 ms.

7.8.28 Register 0x26 (INT_4)

This register contains the threshold definition of the high-g interrupt.

0x26	INT_4							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	0	0	0	0	0
Content	*high_th* <7:0>							

Register	Description
high_th <7:0>	High-g interrupt trigger threshold Scaling of 1 LSB of *high_th*: 2 g-range: threshold = *high_th* <7:0> · 7.81 mg 4 g-range: threshold = *high_th* <7:0> · 15.63 mg 8 g-range: threshold = *high_th* <7:0> · 31.25 mg

7.8.29 Register 0x27 (INT_5)

This register contains the definition of the number of samples to be evaluated for the slope / any-motion interrupt and the no-motion / slow-motion interrupt trigger delay.

0x27	INT_5							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*slo_no_mot_dur* <5:0>						*slope_dur* <1:0>	

Register	Description
slow_no_mot_dur <5:0>	Function depends on whether the slow-motion or the no-motion interrupt function has been selected via *slo_no_mot_sel*. **Slow-motion interrupt function (slo_no_mot_sel = 0):** *N* = *slo_no_mot_dur* <1:0> +1 consecutive slope data points must be above the slow-motion threshold (*slo_no_mot_th*) in order to trigger the interrupt. **No-motion interrupt function (slo_no_mot_sel = 1):** *slo_no_mot_dur* <5:0> defines the time for which no slope data points must exceed the no-motion threshold (*slo_no_mot_th*) in order to trigger the interrupt. The delay time in seconds may be calculated with the following equations. *slo_no_mot_dur* <5:4> = 00 delay time = *slo_no_mot_dur* <3:0> + 1 *slo_no_mot_dur* <5:4> = 01 delay time = *slo_no_mot_dur* <3:0> · 8 + 40 *slo_no_mot_dur* <5> = 1 delay time = *slo_no_mot_dur* <4:0> · 8 + 88
slope_dur <1:0>	The slope / any-motion interrupt triggers if *N* = *slope_dur* <1:0> + 1 consecutive slope data points are above the slope / any-motion interrupt threshold *slope_th*.

7.8.30 Register 0x28 (INT_6)

This register contains the threshold definition of the slope / any-motion interrupt.

0x28	INT_6							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	1	0	0
Content	*slope_th* <7:0>							

Register	Description
slope_th <7:0>	Slope / any-motion interrupt trigger threshold Scaling of 1 LSB of *slope_th*: 2 g-range: threshold = *slope_th* <7:0> · 3.91 mg 4 g-range: threshold = *slope_th* <7:0> · 7.81 mg 8 g-range: threshold = *slope_th* <7:0> · 15.63 mg

7.8.31 Register 0x29 (INT_7)

This register contains the threshold definition of the no-motion / slow-motion interrupt.

0x29	INT_7							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	1	0	0
Content	*slo_no_mot_th* <7:0>							

Register	Description
slo_no_mot_th <7:0>	No-motion / slow-motion interrupt trigger threshold Scaling of 1 LSB of *slo_no_mot_th*: 2 g-range: threshold = *slo_no_mot_th* <7:0> · 3.91 mg 4 g-range: threshold = *slo_no_mot_th* <7:0> · 7.81 mg 8 g-range: threshold = *slo_no_mot_th* <7:0> · 15.63 mg

7.8.32 Register 0x32 (PMU_SELF_TEST)

This register contains the settings for the sensor self-test configuration and trigger.

0x32	PMU_SELF_TEST							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*					*self_test_sign*	*self_test_axis* <1:0>	

Register	Description
self_test_sign	Sign of the self-test excitation is 1: positive 0: negative
self_test_axis <1:0>	Selects the axis to be self-tested 00: self-test disabled 01: x-axis 10: y-axis 11: z-axis When a self-test is performed, only the acceleration data readout value of the selected axis is valid; after the self-test has been enabled, a delay of at least 50 ms is necessary for the read-out value to settle.
reserved	Write 0

7.8.33 Register 0x34 (BGW_WDT)

This register contains settings for the TWI watchdog timer.

0x34	BGW_WDT							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*					*i2c_wdt_en*	*i2c_wdt_sel*	*reserved*

Register	Description
i2c_wdt_en	Watchdog timer at the SDA pin in TWI mode 0: disable 1: enable
i2c_wdt_sel	Watchdog timer period 0: 1 ms 1: 50 ms
reserved	Write 0

7.8.34 Register 0x36 (OFC_CTRL)

This register contains control signals and configuration settings for the fast offset compensation.

0x36	OFC_CTRL							
Bit	7	6	5	4	3	2	1	0
Read/Write	W	W	W	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*offset_reset*	*cal_trigger* <1:0>		*cal_rdy*	*reserved*			

Register	Description
offset_reset	The values of all offset compensation registers (0x38 to 0x3A) are 0: kept 1: reset to 0
offset_trigger <1:0>	Trigger fast offset compensation 00: disabled 01: x-axis 10: y-axis 11: z-axis The offset compensation must not be triggered when cal_rdy is 0.
cal_rdy	Offset compensation is 0: in progress 1: ready to be retriggered
reserved	Write 0

7.8.35 Register 0x38 (OFC_OFFSET_X)

This register contains the offset compensation value for x-axis acceleration readout data.

0x38	OFC_OFFSET_X							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*offset_x <7:0>*							

Register	Description
offset_x <7:0>	Offset value which is subtracted from the internal filtered and unfiltered x-axis acceleration data The offset value is represented in two's complement notation with the following mapping: +127 LSB → +0.992 g 0 LSB → 0 g -128 LSB → -1 g offset_x <7:0> is generated automatically after triggering the fast offset compensation for the x-axis. However, it may also be written directly by the user.

7.8.36 Register 0x39 (OFC_OFFSET_Y)

This register contains the offset compensation value for y-axis acceleration readout data.

0x39	OFC_OFFSET_Y							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*offset_y <7:0>*							

Register	Description
offset_y <7:0>	Offset value which is subtracted from the internal filtered and unfiltered y-axis acceleration data The offset value is represented in two's complement notation with the following mapping: +127 LSB → +0.992 g 0 LSB → 0 g -128 LSB → -1 g offset_y <7:0> is generated automatically after triggering the fast offset compensation for the y-axis. However, it may also be written directly by the user.

7.8.37 Register 0x3A (OFC_OFFSET_Z)

This register contains the offset compensation value for z-axis acceleration readout data.

0x3A	OFC_OFFSET_Z							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*offset_z <7:0>*							

Register	Description
offset_z <7:0>	Offset value which is subtracted from the internal filtered and unfiltered z-axis acceleration data The offset value is represented in two's complement notation with the following mapping: +127 LSB → +0.992 g 0 LSB → 0 g -128 LSB → -1 g offset_z <7:0> is generated automatically after triggering the fast offset compensation for the z-axis. However, it may also be written directly by the user.

8 Safety Concept

Not applicable.

9 Functional and Lifetime Qualification Test Plan

The SMA131 passed the following qualification: AEC-Q100 grade 3.

10 Disclaimer

In order to ensure proper functionality during operation, it is the responsibility of the customer to evaluate:

- The proper function of the sensor in the overall system.
- The mechanical stability of each system design including the sensor.
- The electrical stability, e.g. power supply and EMC, of each system design including the sensor.

Safety and warning notes

Please note that the sensor may be seriously damaged or sensor performance might be influenced by:

- Exceeding the maximum operating conditions. The sensor must be discarded when exceeding these limits.
- Electrostatic discharge. A proper ESD environment during handling and processing of the sensor has to be in place.
- Exceeding the qualification reflow profile. The maximum soldering profile as well as the maximum number of reflow cycles must be observed.
- Exceeding the mission profile: In case a different mission profile than the referred one shall be applied, it needs to be verified whether this profile is still covered by the qualification.
- Improper mechanical connection between the sensor and the PCB and any measure that alters the mechanical stress imposed on the sensor (such as, e.g. soldering, potting, coating, overmolding, etc.). Any measure on application level is considered to be application specific and has to be chosen with care by and in responsibility of the customer

Target market: The product is described by Bosch for the intended application (cf. Chapter 1) and released on the basis of the legal and normative requirements relevant to the Bosch product for use in the following target markets as follows:

The sensor complies with all statutory regulations regarding restriction of hazardous substances and recyclability which are in the scope of IMDS, insofar as such restrictions of hazardous substances and recyclability are regarded, the target market of the sensor is worldwide.

Functional Safety: Bosch points out that the system/product does not implement any ASIL-classified requirements (in the sense of ISO 26262). Therefore, it has not been approved by Bosch for applications in which Bosch delivered system/product has an ASIL related (above QM) role.

This implies the following limitations:

- The SMA131 must not be used if it influences safety goals with ratings higher than ASIL QM. Safety goals are defined in the overall system.
- Bosch cannot provide any quantitative failure analysis (e.g. FTA or FMEDA) for the SMA131.
- The SMA131 does not provide a CRC to check communication errors within a SPI/I2C frame.
- The SMA131 does not provide error flags to detect malfunctions of the ASIC.

Repair of the product is not possible. Manual soldering of sensors is not permitted.
Sensors must not be handled as bulk goods.
Sensors with visible damages (housing, connectors, pins, etc.) and sensors which might have exceeded the absolute maximum ratings must not be mounted in the vehicle. These sensors must be scrapped.

Data Security: The sensor only contains the explicitly stated characteristics for product, data and information security. It is the responsibility of the system integrator to verify and validate on system level, if the stated characteristics comply with and fulfil the requirements of the product.

Assessment of Products Returned from Field: Returned products are considered good if they fulfill the specifications / test data for 0-mileage and field listed in this document.

Due to the measurement principle, the sensor is sensitive to mechanical disturbances, such as shocks, vibrations or stress. Therefore, the printed circuit board (PCB) has to be designed in such a way, as to suppress any of these influences and ensure the proper functionality in each application.

The sensor elements have to be protected against extreme shock loads such as e.g. hammer blows on or next to the sensor elements, vibrations of a power wrench when fixing bolts, dropping of the sensor elements onto hard surfaces, etc.. Sensor modules which have been dropped must not be used and have to be scrapped. We recommend the avoidance of g-forces beyond the maximum rating during transport, handling and mounting of the sensors resulting in a defined and qualified installation process. As the sensor is sensitive to mechanical stress, any bending or torsion of the PCB close to the sensor, e.g during forcing in, has to be avoided.

Engineering Samples: Engineering samples are marked with (e) or (E). Samples may vary from the valid technical specifications of the series product contained in this data sheet. Therefore, they are not intended or fit for resale to third parties or for use in end products. Their sole purpose is internal client testing. The testing of an engineering sample may in no way replace the testing of a series product. Bosch assumes no liability for the use of engineering samples. The purchaser shall indemnify Bosch from all claims arising from the use of engineering samples.

11 Changes

This TPD is on basis of SMA131 Technical Customer Documentation (TCD) 1 279 929 852 Rev. 3.0.

12 Table of Figures